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Industrial Policy through the CHIPS and Science Act

A Preliminary Report

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I. Introduction

The US government launched a new wave of semiconductor industrial policy projects soon after a chip [shortage](#) crimped American manufacturing during the pandemic amid escalating geopolitical tensions with China. The White House and Congress grew concerned because chips are essential to many other commercial and defense-related industries, and many are made outside the United States, leaving the country vulnerable to supply disruptions. When they enacted the 2022 [CHIPS and Science Act](#), one of their key aims was to boost production of advanced chips on US territory and to induce semiconductor firms based in the United States and in friendly and allied jurisdictions (especially Japan, South Korea, and Taiwan) not to expand production in China. (CHIPS stands for Creating Helpful Incentives to Produce Semiconductors.) Goals for domestic production included enhancing economic and national security, reducing US reliance on imported chips, and producing 20 percent of global leading-edge logic chips by 2030.

Industrial policy can be broadly defined as government intervention through subsidies (grants, low-interest loans, preferential taxes) and trade restrictions (usually tariffs or quotas on imports) designed to bolster particular sectors or technologies. The CHIPS and Science Act relies heavily on cash subsidies and tax credits. Division A of the legislation authorizes subsidies to semiconductor firms, Division B provides a range of research and development (R&D) subsidies, and Division C authorizes funding for Supreme Court security.

This report assesses the effectiveness so far of Division A, hereafter called the CHIPS Act, in achieving the goals listed above. It aims to help policymakers consider whether additional subsidies to extend the CHIPS Act mandate will be warranted once current funding runs out. In a forthcoming paper, Martin Chorzempa explores the success of US government initiatives, under the CHIPS Act and other legislation, in limiting Chinese access to advanced semiconductor technology.¹

Overall, we find the following:

- The CHIPS Act will sharply increase production of advanced semiconductors on US territory. This will enhance national security to the extent that it boosts the domestic supply of chips, reducing the risk of future shortages. But more production might not provide the best security for the money. Lawmakers

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1 Martin Chorzempa, Effectiveness and costs of US export controls on semiconductors (Washington: Peterson Institute for International Economics, forthcoming).

deliberating the act did not consider alternative ways of spending \$200 billion to ensure adequate chip supplies.

- Increased domestic semiconductor production may reduce but not eliminate US reliance on imported chips. US imports of chips, particularly “mature” or “legacy” types, will likely remain substantial.
- Additional subsidies likely will be needed to achieve the goal of producing 20 percent of global leading-edge logic chips in the United States by 2030. Even then, significant challenges remain.
- Job creation has frequently been touted as a benefit, if not a top goal, of the CHIPS Act. We estimate that approximately 93,000 temporary construction jobs and 43,000 permanent jobs will be created, at an average subsidy cost of \$185,000 per job per year—about twice the average annual salary of US semiconductor employees.

Additionally, it is worth noting that in earlier phases of the semiconductor industry, subsidies clearly accelerated technological advancement, but the same cannot be said with confidence about the post-2020 burst of subsidies in the US and competing jurisdictions.

HISTORICAL US EXPERIENCE

Industrial policy has a long history in the United States. The first secretary of the US Treasury, Alexander Hamilton, is widely considered to be the pioneer champion of US industrial policy. In his acclaimed 1791 *Report on the Subject of Manufactures*, Hamilton outlined a strategy to protect and develop fledgling industries through a series of protectionist subsidies and tariffs. George Washington, the first president of the United States, endorsed this plan. This “Hamiltonian” tradition of industrial policy has been repeated in various forms throughout US history, most notably through Henry Clay and John Quincy Adams’ vision of an “American system”—an economic plan that included high tariffs to protect American industries and generate revenue for the federal government, a national bank to stabilize US currency and rein in risky state banks, and transportation infrastructure to connect the country. From the 1820s to the 1930s, US industrialization entailed average applied industrial tariffs [greater than 30 percent](#), among the highest in the world and justified by the Hamiltonian tradition.

Two other traditions of US industrial policy can also be attributed to the founding fathers: the “[Franklinian](#)” tradition (which focuses on promoting research and infrastructure rather than protecting particular industries, attributed to Benjamin Franklin) and the “[Madisonian](#)” tradition (which focuses on using antitrust and kindred regulations to create competitive markets, attributed to James Madison). During the 19th century, in addition to episodic high tariffs on manufactured imports, the federal government gave substantial subsidies (often in the form of land grants) to railways and canals, technological pioneers of their day. Federal funding for science research, such as the Manhattan Project to develop the atomic bomb during World War II, the Defense Advanced Research Projects Agency (DARPA), and the Apollo program to win the space race against the Soviet Union, are all examples of Franklinian industrial policy. On the

other hand, laws to prevent monopolies and oligopolies, such as the Sherman Antitrust Act, the Clayton Antitrust Act, the Federal Trade Commission Act, the Packers and Stockyards Act, and the Hepburn Act, are all examples of the Madisonian tradition.

American industrial policy throughout the latter half of the 19th century had a strong Franklinian streak. In the 1860s President Abraham Lincoln began building the [transcontinental railroad](#)—at the time, the most ambitious civil engineering undertaking in the world—which was critical to link America’s emerging engineering sector with its established agro-industrial sector. State-sponsored and federally supported research and development programs began at the same time, starting first in agriculture (with land grant colleges) and [later expanding](#) into areas such as animal husbandry, agricultural chemistry, forestry, and mining. In the early 20th century American industrial policy stressed the Hamiltonian tradition: The federal government used airmail fees to subsidize the civilian aviation industry, and government procurement was used to establish both the US aircraft industry and the advanced chemical sector.

In the 1930s and 1940s, after a burst of measures to counter the Great Depression, federal industrial policy increasingly responded to external threats. President Franklin D. Roosevelt’s New Deal programs not only sought to ensure economic recovery but also to strengthen the US defense industry during World War II. In addition to the Manhattan Project, the US government subsidized a number of fundamental innovations, including missile technology, civilian nuclear power, computers, transistors, and satellites. During the Cold War, US industrial policy was driven by competition with the Soviet Union, resulting in research breakthroughs credited with paving the way for the modern internet and the Global Positioning System (GPS), among others. Airports and highways, funded by cash subsidies, were added to the mix. Favored industrial sectors also were shielded from competitive imports.

Somewhat paradoxically, industrial policy was implemented even at times when the US government was ideologically hostile. President Ronald Reagan, for example, was a staunch opponent of industrial policy but nevertheless protected US steel, auto, and motorcycle industries from import competition and spurred the US semiconductor industry through the Semiconductor Manufacturing Technology (Sematech) consortium to upgrade US chip manufacturing processes.² Still, industrial policy fell out of favor in the 1980s and 1990s with the advent of the “[Washington Consensus](#),” a set of 10 economic policies that included maintaining fiscal discipline, reforming tax policy, liberalizing trade, and reordering public spending priorities from industrial subsidies to health and education expenditures.

In 2022 [Hamiltonian industrial policy](#) was back in vogue. The US Congress passed both the Inflation Reduction Act, with a projected cost of \$783 billion (private estimates are higher), and the CHIPS and Science Act, with an overall authorized budget of \$278 billion. The CHIPS part of the act (hereafter the CHIPS

2 The US military was also a big purchaser of chips. But according to PIIE senior fellow Alan Wolff, a knowledgeable observer, the military concentrated on prior-generation chips and wanted them to be radiation hardened, which was a burden to the industry. More beneficial was the development of transistors through government purchases. US formation of the Sematech consortium was largely a reaction to Japanese sponsorship of joint research through Nippon Telephone and Telegraph Corporation and the Ministry of Industry and Technology.

Act), with an emphasis on economic and national security, has an authorized and appropriated budget of \$50 billion, plus another \$100 billion or more in tax credits.

2021 PIIE REPORT: SCORING 50 YEARS OF INDUSTRIAL POLICY, 1970–2020

In 2021 the Peterson Institute for International Economics (PIIE) published a detailed report authored by Gary Clyde Hufbauer and Euijin Jung, *Scoring 50 Years of Industrial Policy, 1970–2020*, analyzing 18 industrial policy ventures. Some of the ventures had two phases, so the total count is 21 projects. Most were carried out by the federal government, but 3 were state projects. Nearly all 18 projects aspired to create an industry, or develop a technology, that could flourish in a competitive world market. National security was the object of only one program: DARPA. But in the Hufbauer and Jung report, even DARPA was evaluated on economic criteria, not its substantial contribution to national security. The top-line summary suggests that past episodes of industrial policy often failed. In some instances, trade restrictions were invoked to revive the fortunes of lagging industries, without success. In other instances, the wrong technology was promoted. On the whole, research-intensive projects fared the best.

The 21 projects were grouped into three categories: industries supported by trade restrictions (tariffs or quotas), industries receiving government subsidies (grants, low-interest loans, or tax preferences), and subsidized projects with a dominant R&D component. The common economic framework analyzed three metrics for each project: whether the designated industry or technology became competitive by world market standards, how many jobs were created (or saved) in the target industry and the cost per job, and whether the project advanced the technological frontier. For each metric, outcomes were graded on a four-letter scale of A to D.

Figure 1 below summarizes the report's findings. Industrial policy in eight cases took the form of trade restrictions. Of 21 projects, the report found slightly more outright failures (D grades) than clear successes (A grades) in terms of meeting world competition. The score was nine failures to eight successes, with four intermediate cases. In terms of creating (or saving) jobs at an acceptable cost, there were more successes than outright failures, scoring nine to seven. The strongest contribution of the 21 industrial policy projects was in advancing the technological frontier, with 12 clear successes (A grades).³

Three cases among the 21 projects are most closely related to objectives of the CHIPS Act: both the antidumping and market-opening phases of semiconductor trade restrictions and R&D support for the Sematech consortium. Antidumping duties against Japanese semiconductor imports did little to boost the US semiconductor industry.⁴ However, for a time, Japan's agreement to open

3 Other knowledgeable observers might well assign different grades to the cases. Alan Wolff, for example, argues that the Sematech consortium improved US competitiveness for several years, and that the steel outcome would have been better if the United States had launched antitrust cases against Japanese and European firms.

4 The antidumping cases were highly selective. Micron Technology brought cases against Japanese dynamic random access memory (DRAM) chips, and Intel brought a case against erasable, programmable read-only memory (EPROM) chips.

Figure 1

US industrial policy has worked best when used to fund industry research and development

Scorecard for 18 US industrial policy episodes, 1970–2020

	Did the industry become more competitive?	Were jobs saved or created?	Did industry technology advance?
Trade measures			
Steel	D	D	D
Textiles & apparel	D	D	C
Automobile assembly	A	A	A
Automobile parts	B	C	A
Semiconductors (antidumping phase)	D	D	C
Semiconductors (foreign market opening phase)	B	A	A
Solar panels (tax credits)	D	A	A
Solar panels (trade protection)	D	B	D
Subsidies			
Synthetic Fuels Corporation	D	D	D
Solyndra Corporation	D	D	D
Crescent Dunes	D	D	D
Mercedes-Benz in Alabama	A	A	B
Chrysler bailout in 1980	A	A	A
Foxconn in Wisconsin	C	B	D
Research and development			
Defense Advanced Research Projects Agency (DARPA)	A+	A+	A+
Renewable energy	D	A	A
Sematech	C	B	A
Florida Biotech Center	A	D	A
Advanced Technology Vehicles Manufacturing Loan Program	A	B	A
Operation Warp Speed	A	A	A
North Carolina Research Triangle Park	A	A	A

Source: Gary Clyde Hufbauer and Euijin Jung, *Scoring 50 years of US Industrial Policy, 1970–2020*, PIIE Briefing 21-5 (<https://www.piie.com/research/piie-charts/2021/us-industrial-policy-has-worked-best-when-used-fund-research-and>).

its own semiconductor market to US exports did improve the fortunes of US chip firms.⁵ Federal R&D support for the Sematech consortium was an effort to upgrade US chip manufacturing processes through shared experience of the consortium members (leading semiconductor firms of the day). Manufacturing technology was improved, but US firms did not become more competitive relative to South Korean and Taiwanese firms, which were making great strides at the same time.⁶ It is worth noting that the South Korean chip industry got a start partly due to government research institutes but received few direct subsidies, whereas the Taiwanese industry benefited from early but relatively modest subsidies.

INDUSTRY CHARACTERISTICS

Semiconductors come in many different shapes, sizes, and functions. The Semiconductor Industry Association (SIA) lists [63 types](#) of chips. They are arranged in [nine chip categories](#): logic, memory, analog, microprocessor unit, optoelectronic, discrete semiconductor, microcontroller unit, sensor, and digital signal processor.

[Statista](#) further compresses the variety into four categories and reports their share of total global revenue (\$610 billion) in 2022: integrated circuits (83 percent; \$504 billion), optoelectronics (8 percent; \$47 billion), discrete semiconductors (6 percent; \$37 billion), and sensors and actuators (4 percent; \$23 billion). Interested users can purchase Statista's 2027 market forecasts for \$995.

In today's world, six jurisdictions⁷ dominate semiconductor design and production: the United States, Japan, South Korea, Taiwan, China, and the European Union. These are commonly called the Big 6. Smaller production sites, often through subsidiaries of Big 6 firms, exist in countries such as Israel, Malaysia, and Singapore.

Advances in semiconductor technology are often scaled by a measure of miniaturization within the chip, expressed in nanometers (nm). One nanometer is one-billionth of a meter (a human hair is about 60,000 nm wide). The smaller the number of nanometers, the greater the density of connections within a chip. However, the nanometer measure does not refer to the width of connections. In 2000 a [90 nm chip](#) was the frontier; in 2024 a [2 nm chip](#) is the frontier.

Turning to economic characteristics, the industry supply chain has three major components: chip design; chip manufacture (foundries); and chip assembly, testing, and packaging (ATP). Wage cost differentials drive nearly all ATP work to Asia. For the moment, US firms are design leaders. Locational competition is [most evident](#) for chip manufacturing.

5 The agreement prevented dumping in any market (not only the US market) by individual Japanese companies. However, the main problem faced by US firms was vertical integration between Japanese chip producers and Japanese chip purchasers. To some extent, this was overcome by Japan's agreement to purchase US chips.

6 US semiconductor firms rejected the proposal, offered by IBM vice president Sandy Kane, to create a jointly owned domestic foundry, US Memories. Evidently, they preferred to outsource production to the Asian firms.

7 The term *jurisdictions* is used because neither the European Union nor Taiwan is a country.

Sharp distinctions must be made between three national metrics of the supply chain: the global revenue of firms headquartered in a country; the sales of semiconductors to the national market; and the capacity of foundries, or “fabs,” in national territory.

As table 1 (panel a) shows, US-headquartered firms are absolutely dominant in terms of global revenue, accounting through far-flung operations for nearly half of world sales. Control of design explains US dominance. Illustrative is the way Nvidia has [swept the world](#) with graphics processing units (GPUs) that enable artificial intelligence (AI). US firms are also exporters of advanced chips made in East Asian foundries according to US specifications (like GPUs), exported to the US design firms (like Nvidia), and then reexported to global destinations. Those facts go a long way to explain why SIA is a [valiant supporter](#) of free trade.⁸ Viewed from the standpoint of headquartered firms, the US industry and its congressional supporters have no complaints about America’s standing in the world semiconductor league. Their complaint is centered on the absence of manufacturing capacity in US territory.

China leads the world in terms of semiconductor sales to its market, accounting for almost half of sales to the Big 6 semiconductor jurisdictions, as shown in table 1 (panel b). Domestic sales, of course, reflect the size of domestic consuming industries. China is a huge producer of consumer electronics and automobiles—both major chip users—and hence a leading chip importer. China’s dominance in terms of semiconductor sales within its domestic market was not a motivation for the CHIPS Act, though China’s technological capabilities were an important driver.

The lagging capacity of foundries on US territory spurred the CHIPS Act. As table 1 (panel c) shows, US foundry capacity, expressed as a share of world capacity, consistently declined after 1990, dropping from [37 percent](#) in that year to 12 percent in 2020. In panel c, capacity is measured by the annual volume of circular wafers of 200 millimeters (mm; about 8 inches) or larger diameter that can be produced by the foundry. Silicon chips have widely varying sizes, so the number of chips on a single wafer can vary from less than 100 to more than 1,000. With the advance of chip design, the cost of new foundries has dramatically escalated. In the 1970s a fab might have cost \$30 million (in 2024 dollars), whereas in the 2020s the cost could range from [\\$10 billion to \\$20 billion](#). Lithography equipment accounts for a large share of fab cost. The configuration and equipment in an existing foundry [seldom can be reconfigured](#) for the next generation of chips. Instead, a new and more expensive foundry must be built. Meanwhile, the human skills required for foundry work have become more demanding. East Asian firms, especially in South Korea and Taiwan, became adept at constructing and operating foundries and delivering quality chips with low defect rates. US-headquartered firms thus progressively focused on the next generation of chip design and consigned foundry manufacture to East Asia.

The CHIPS Act seeks to reverse industrial history by bolstering foundry construction in the United States, particularly foundries for leading-edge logic

8 SIA also historically opposed foreign subsidies, particularly those given by China. For a detailed account of US policy, see [Wolff’s 2022 paper](#).

Table 1

Characteristics of semiconductor industries in the Big 6 jurisdictions, 2014–23

<i>a. Revenue by headquarter firms (billions of current US dollars)</i>										
Jurisdiction	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
China	13.4	13.4	16.9	20.6	23.4	20.6	22.0	38.9	40.2	37.9
European Union	26.9	30.2	30.5	37.1	42.2	41.2	44.0	50.0	51.7	66.9
Japan	40.3	36.9	33.9	41.2	42.2	41.2	44.0	50.0	51.7	47.4
South Korea	57.1	57.0	74.6	90.7	112.5	78.3	88.1	116.7	109.1	72.7
Taiwan	23.5	20.1	20.3	24.7	28.1	24.7	30.8	44.5	45.9	36.9
United States	171.3	167.6	155.9	189.6	211.0	193.8	207.0	255.7	275.5	264.5
World total	335.8	335.2	338.9	412.2	468.8	412.3	440.4	555.9	574.0	526.9
<i>b. Sales to national markets (billions of current US dollars)</i>										
Jurisdiction	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
China	91.6	98.6	122.4	147.8	170.8	156.0	166.1	205.5	193.7	179.5
European Union	37.5	34.3	32.7	38.3	43.9	39.4	41.0	50.6	58.1	53.1
Japan	34.8	31.1	32.4	36.0	39.7	36.8	38.7	45.5	51.9	48.5
South Korea	n.a.	n.a.	13.7	17.3	20.0	16.4	17.3	20.9	19.8	17.0
Taiwan	n.a.	n.a.	n.a.	n.a.	24.7	20.2	23.7	31.3	30.1	25.7
United States	n.a.	n.a.	44.2	53.2	60.6	54.9	57.7	70.6	80.5	70.2
<i>c. 200+ millimeter commercial semiconductor fab capacity in national territory (percent of total world capacity)</i>										
Jurisdiction	1990	1995	2000	2005	2010	2015	2020	2022	2025F	2030F
China	0	0	1	7	11	12	18	24	24	22
European Union	44	24	25	17	13	11	7	8	8	8
Japan	17	19	16	21	18	15	18	17	15	15
South Korea	0	12	13	14	15	18	18	17	18	19
Taiwan	2	15	22	21	22	24	19	18	18	17
United States	37	27	19	14	13	13	12	10	11	13

n.a. = not available; F = forecast

Sources: Boston Consulting Group and Semiconductor Industry Association (SIA) report (https://www.semiconductors.org/wp-content/uploads/2024/05/Report_Emerging-Resilience-in-the-Semiconductor-Supply-Chain.pdf); SIA Factbook, 2015–24 (<https://www.semiconductors.org/resources/factbook/>); Statista (<https://www.statista.com/outlook/tmo/semiconductors/worldwide?currency=USD>).

chips. The joint forecast of the Boston Consulting Group (BCG) and SIA sees US foundries reaching 13 percent of world capacity in 2030.

US-headquartered firms account for around two-thirds of world semiconductor R&D, as shown in table 2. This largely explains US preeminence in chip design. Authors of the CHIPS Act saw no call to provide additional R&D tax credits for the semiconductor industry. Yet the latest [Organization for Economic Cooperation and Development \(OECD\) report](#) puts the United States near the

Table 2

Semiconductor R&D expenditures by the Big 6 jurisdictions, 2014–23 (billions of current US dollars)

Jurisdiction	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
China	1.2	1.2	1.6	1.6	2.0	1.7	1.5	3.0	3.1	2.9
European Union	4.1	4.6	4.6	5.2	5.9	6.3	7.5	7.5	7.7	9.4
Japan	2.1	1.9	1.8	3.5	3.7	3.5	5.7	4.2	4.3	5.7
South Korea	4.7	4.7	6.1	7.3	8.2	6.0	7.4	10.6	9.9	6.9
Taiwan	2.2	1.9	1.9	2.4	2.8	2.5	3.3	4.9	5.1	4.1
United States	35.0	33.8	33.9	35.9	38.7	39.8	44.0	50.2	58.8	59.3
Rest of world	0.5	1.4	1.0	0.4	0.5	0.7	0.2	0	0	0
World total	49.7	49.5	50.8	56.4	61.7	60.6	69.6	80.3	88.9	88.2
<i>US R&D as percent of total world R&D</i>	70.4	68.3	66.8	63.7	62.7	65.7	63.2	62.5	66.2	67.2

Sources: Semiconductor Industry Association Factbook, 2015–24 (<https://www.semiconductors.org/resources/factbook/>).

bottom of advanced countries in terms of the generosity of its R&D subsidies for large profitable firms. And the Tax Foundation [criticizes the United States](#) for the paucity of R&D tax benefits compared to China. Such comparisons found no traction in the CHIPS Act.

Instead, President Joseph R. Biden and Congress focused on spurring US capital expenditures (capex), largely in foundry construction. Considering the lament over the declining US share of world fab capacity, the capex facts summarized in table 3 may come as a surprise. The table shows global capex by US-headquartered firms, world total semiconductor capex, and capex by all firms (US and foreign firms) on US territory. Since 2014, US-headquartered firms have consistently accounted for around a third of world capex. The dramatic change is in the share of world capex on US territory, by both US and foreign firms. As recently as 2018, that share was under 4 percent. By 2022 the share surged to reach 45 percent of world capex. The surge preceded passage of the CHIPS Act in August 2022. Semiconductor legislation was a lively topic as early as 2020, with a preview contained in defense authorization bills; thus, anticipation helps explain the dramatic lift. Going forward, a central question in evaluating the CHIPS Act is whether the very high percentage of world capex on US territory will be maintained. US territorial capex now far exceeds US-headquartered firm capex worldwide, so continued high investment by East Asian firms on US territory will be essential to maintain the US territorial share of world capex.

There are at least three reasons for the apparent contradiction between lagging US territorial chip capacity (12 percent of world fab capacity in 2020) and robust US territorial capex (45 percent of world capex in 2022). First, the capacity figures reflect the inherited stock of past capex. Judging from capex data before 2019, not much fab capacity was installed on US territory in the first two decades of the 21st century. Second, under East Asian conditions, it is possible to construct substantially more fab capacity with a billion dollars of capex than under US conditions, owing to more experienced construction firms

Table 3

US and world semiconductor capital expenditures, 2014–23 (billions of current US dollars or percent where specified)

Item	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
US HQ capex	18.0	21.6	23.0	24.9	32.7	31.9	30.2	40.4	50.8	48.2
US territory capex	1.1	1.7	1.9	3.0	3.6	7.0	13.9	45.8	81.7	n.a.
World total capex	66.1	65.2	67.8	95.6	106.1	102.5	113.1	153.1	181.7	146.6
US HQ capex as percent of world total	27.2	33.1	33.9	26.0	30.8	31.1	26.7	26.4	28.0	32.9
US territory capex as percent of world total	1.7	2.7	2.7	3.1	3.4	6.8	12.3	29.9	44.9	n.a.
US territory capex as percent of US HQ capex	6.1	8.0	8.1	11.9	11.1	21.8	46.1	113.3	160.7	n.a.

n.a. = not available

Notes: *US HQ capex* refers to the capital expenditure conducted by firms that are headquartered in the United States, no matter the physical location of that capex. Conversely, *US territory capex* counts all capital expenditures that are spent on the US territory, no matter where the companies are headquartered.

Sources: Semiconductor Industry Association *Factbook*, 2015–24 (<https://www.semiconductors.org/resources/factbook/>); Statista (<https://www.statista.com/study/136376/tech-hardware/>); RSM US (<https://rsmus.com/insights/industries/manufacturing/us-semiconductors-an-outlook-of-promise-and-challenges.html>).

and lower wages in East Asia. Third, the reported capacity figures make no adjustment for the complexity and value of individual silicon chips within each wafer. A standard dynamic random access memory (DRAM) chip with 256,000 (256K) bits of memory may cost \$2 each; the latest Nvidia GPU chip will be priced at \$30,000. Trade data summarized later in this report show that chips exported from the United States are significantly more valuable than imported chips in the same detailed product code. Hence, reported capacity figures understate US capabilities, in terms of semiconductor value, relative to other Big 6 producers.

II. Global Subsidies

SUBSIDIES IN THE BIG 6 JURISDICTIONS

Almost from its inception in 1958, the semiconductor industry became an object of national industrial policy, first documented by Thomas R. Howell et al. in a 1988 volume, *The Microelectronics Race*, and [stressed](#) by Laura D'Andrea Tyson and David B. Yoffie in their pioneering 1991 paper “Semiconductors: From Manipulated to Managed Trade.” The National Research Council of the National Academies further documented the prevalence of international industrial policy competition in a [2003 report](#).

In 1965, shortly after the industry was commercialized, Gordon Moore announced “[Moore’s law](#)”—as later formulated, the number of transistors on an integrated circuit (IC) chip would double every two years. Technological advances dramatically increased the market for chips in a wide variety of consumer and industrial products. Each of the [six leading jurisdictions](#)—the United States, Japan, South Korea, Taiwan, China, and the European Union—sought to bolster its industry with public support. The quest for leadership is now heightened by intense geopolitical competition between the United States and China. Added are fresh concerns over [supply chain vulnerability](#) in the wake of the [COVID pandemic](#), an issue summarized by [Chad P. Bown](#). Together, geopolitical competition and supply chain vulnerability informed the economic and national security objectives of the CHIPS Act.

The ensuing parade of industrial policy measures by the Big 6 jurisdictions had [three characteristic features](#). First, the dominant type of subsidy evolved from government purchases, research institutes, and trade protection (which, for major producers other than China, [practically disappeared](#) by 2000) to cash grants, tax credits, and kindred measures. Second, over time these measures acquired a larger footprint, signaling more intrusive government policy. Third, measures introduced by any one of the six leaders became a rationale for the others to ramp up their own interventions. The global semiconductor industry is now traveling a path whereby industrial policy [in one country](#) triggers [fresh installments](#) in competing countries. Former US Treasury Secretary Lawrence Summers [famously said](#), “I believe that the best generals are the ones who hate wars most, and I believe the best industrial policy experts are the ones who hate it most. The problem is that the only people who talk about industrial policy are the ones who love it and are looking for a reason to do it.” This roughly summarizes six decades of semiconductor industrial policy in the Big 6 jurisdictions.

Industrial policy is expressed in several ways, some difficult to quantify. The better-known measures, once tariffs were phased out, include semiconductor training and R&D in research institutes and national universities, consolidation of domestic semiconductor firms, mandated cooperation between private firms, obligatory government and private procurement of chips from domestic suppliers, occasional high tariffs and penalty duties, preferential tax rates and tax credits for R&D outlays and plant capex, and outright grants and favorable loans for semiconductor firms. Many of these measures are quantified in a careful [OECD paper](#) covering the years 2014–18.

The next several sections, jurisdiction by jurisdiction, sketch the major themes of central government industrial policy with a focus on tax preferences, grants, and loans—measures that dominate the current phase of national competition. These sketches rely on published data. Among useful sources is a 2023 [Congressional Research Service report](#). Once the CHIPS Act became law, the US Department of Commerce assembled expert teams to evaluate and monitor subsidies currently offered by other Big 6 jurisdictions. Valuable comparative data have no doubt been collected, but so far the data have not been made public.

Readers may ask, “Where was the World Trade Organization (WTO) as the subsidy bonanza unfolded?” Apart from a few antidumping and countervailing duty cases brought by the United States and European Union against Japan, Korea, and Taiwan, the WTO was silent. According to Alan Wolff, SIA’s trade counsel from 1980 until 2017, SIA campaigned against “regional support” (meaning subsidies) in the World Semiconductor Council and the Government and Authorities Meeting on Semiconductors. However, the administration of President Donald J. Trump put the WTO Appellate Body out of business, and that pretty much [ended any effort](#) to invoke WTO rules against Chinese (or other) subsidies. Meanwhile, successful chip firms headquartered in the Big 6 jurisdictions and with plants located worldwide benefited from the subsidy parade. [Bown](#) digs into the details of WTO interaction with industrial policy, but more to the point is a [PIIE podcast](#) that reveals how subsidies since the global financial crisis of 2008–09 have swamped the WTO rulebook.

In his engaging and influential book *Chip War*, Chris Miller recounts the persona, tech milestones, and government policies that created semiconductor firms in each of the six leading jurisdictions. [Bown](#) and [Wolff](#) provide less passionate but more detailed accounts of public policy. In contrast to the pioneering essay authored by [Tyson and Yoffie](#) in 1991, Miller emphasizes the military dimension. He details the decisive role of semiconductors in the first and second cold wars, the two Iraq wars, and future battlefields of drones and robots. *Chip War* was published on October 4, 2022, just two months after President Biden signed the CHIPS and Science Act on August 9. In the eyes of industry and congressional sponsors, Miller’s account of brutal competition between US and Chinese chip industries fully justifies robust national security goals in the CHIPS Act.

The brief country sketches that follow draw on fuller histories by Miller and others. Of special note is the January 2024 [working paper](#) by Bown and Dan Wang and the May 2024 report issued by BCG and SIA, [Emerging Resilience in the Semiconductor Supply Chain](#). Countries not covered in the sketches below—

for example, Malaysia and Singapore—are essentially outposts for firms based in the leading jurisdictions. The principal attractions of these outposts are low taxes and (at one time) cheap labor.

UNITED STATES

Among guiding lights for the [industry's creation](#) in the late 1940s and early 1950s were Nobel laureates and creative entrepreneurs: William Shockley, Jack Kilby, Robert Noyce, and Gordon Moore. The year 1958 saw the first chapter of US industrial policy when the two corporate pioneers of ICs, Fairchild Semiconductor and Texas Instruments, were supported by Pentagon and National Aeronautics and Space Administration (NASA) contracts. For several years, brisk Cold War demand for chips for defense and space purposes took most of the industry's output, and the military paid high prices. Once Fairchild and Texas Instruments were soundly established, the Pentagon's goal shifted from nourishing the industry to developing the best chips for military hardware.

Industry leader Robert Noyce saw the growth potential of serving nonmilitary uses if chip prices could be slashed. In this quest, firms such as Texas Instruments, IBM, and Intel spent substantial funds on R&D that advanced technology, lowered prices, and dramatically expanded chip sales. In 1965 most ICs were made for military hardware, but by 1968 some 75 percent of chips were sold for commercial applications. In subsequent decades, the commercial history of the chips industry illustrated Say's law—namely, that supply creates its own demand. Ever-improving capabilities opened ever-larger markets.⁹ The latest spectacular case is Nvidia's GPU chips driving the market for AI.

During the long Cold War between the United States and the Soviet Union, the Soviet Union did its best to copy US chip technology, but it never caught up—owing to the combination of Moore's law, extensive R&D by private US firms, and US federal support. The second chapter of US industrial policy commenced in 1976 when DARPA started awarding grants for research labs, universities, and individual academics to find ways of miniaturizing chips. DARPA R&D funding was modest, but it created the chip design software industry, which to this day remains the stellar US component of the semiconductor industry.

The third chapter of US industrial policy was a direct response to Japanese industrial policy. By the 1980s, DRAM chips, invented by Intel in 1970, were big sellers. Japanese firms excelled in producing DRAMs at low prices with better defect rates than US firms (0.02 versus 0.09), and they soon captured a large share of the US market. The next section sketches Japan's industrial policy. In 1978, at the urging of Silicon Valley and other industries, and well before the United States took direct action against Japan, the US capital gains tax rate was cut from 49 percent to 28 percent, a major incentive to venture capitalists. In 1984, to limit intellectual property losses, Congress passed the Semiconductor Chips Protection Act. Shortly after, in 1986, the [focused US response](#) against Japan had [two parts](#): antidumping cases, which were resolved by a price-fixing

⁹ As originally formulated by Jean-Baptiste Say, it was income generated by production that created demand. In the case of chips, it is improved technology that creates demand.

arrangement,¹⁰ and the Semiconductor Trade Agreement (STA), a market-opening agreement by which Japan raised the US share of its DRAM market from 10 percent to 20 percent. The price-fixing arrangement was some help to Micron and Motorola but not so much to other US firms. However, the market-opening agreement gave broad benefit to the US industry. In addition to trade remedy cases against Japan, [smaller cases](#) were brought in the 1990s against South Korea and Taiwan. In 1996 WTO members signed the Information Technology Agreement, calling for [zero tariffs](#) on imports of semiconductors and computer parts. According to Wolff, this was preceded by a duty-free agreement on chips between the United States, Canada, and Japan.¹¹

The fourth chapter of US industrial policy was the creation of the Sematech consortium in 1987, which lasted until 1997 and was then taken over on a reduced scale by New York State. Sematech was initially funded half by DARPA (\$100 million annually for 10 years) and half by 14 leading US chip firms. Noyce was recruited to lead Sematech. The origins of its name—Semiconductor Manufacturing Technology—speak to its purpose: raise US chip production technology to meet or beat Japanese practice. An objective highlighted by Noyce was to improve US advanced lithography machines, which embed circuits on silicon. Nevertheless, the Geophysical Corporation of America (GCA), the leading US lithography firm, did not survive stiff competition from Nikon, Canon, and Advanced Semiconductor Materials Lithography (ASML). Today the Dutch firm ASML dominates the market for these complex machines, with the latest versions costing up to \$300 million per copy. But Sematech somewhat improved US manufacturing methods through shared technology between consortium members.¹²

The CHIPS Act opens the fifth chapter of US industrial policy. A congressional report [summarizes](#) the legal text. With a headline cost of \$76 billion, the CHIPS Act authorizes \$39 billion for production grants and \$11 billion for R&D. Within the \$39 billion for production grants, some \$6 billion is authorized as the subsidy cost of concessional loans, calculated at 8 percent of their face value (implying up to \$75 billion of concessional loans). In addition, a 25 percent investment tax credit is authorized for projects launched before January 2027 ([unrealistically budgeted](#) at just \$26 billion but likely to reach \$100 billion). All told, the CHIPS Act exceeds by an order of magnitude [prior individual industrial policy ventures](#) over the past 50 years. [Setting the stage](#) for the CHIPS Act were [influential reports](#) by BCG and SIA.

Economic and national security concerns inspired the CHIPS Act. The act requires the secretary of commerce [to determine](#) “that the project to which the application relates is in the economic and national security interests of the United States” before approving a grant or concessional loan. Accordingly, the Department of Commerce published a [guidebook](#) explaining its approach to national security. The guidebook informs the work of the [CHIPS Program Office](#) (CPO), which consists of approximately 150 newly recruited professionals who

10 Price-fixing terms were specified for each individual Japanese chip firm and applied to sales in all markets.

11 Private communication from Alan Wolff.

12 As reported by [Hufbauer and Jung](#), a 1996 article by [Douglas A. Irwin and Peter J. Klenow](#) reached a more negative conclusion about the benefits of the Sematech consortium.

provide the commerce secretary with a confidential assessment of the national security merits of each applicant. As detailed later in this report, economic and national security concerns led the Department of Commerce to concentrate grants and loans on “advanced” and “leading-edge” projects. It is important to emphasize that the 25 percent [investment tax credit](#)—prospectively the largest subsidy in the CHIPS Act—is *not* conditioned on the economic or national security merits of each qualifying project. The tax credit is available not only to firms that are awarded grants and concessional loans by the Department of Commerce but also to any firm that creates or adds to a semiconductor plant on US territory. On October 23, 2024, the Treasury Department issued [final regulations](#) detailing conditions for firms to receive the investment tax credit.

Postscript: US state subsidies

Pioneers of the semiconductor industry—Shockley, a Nobel laureate; Noyce, founder of Fairchild Semiconductor and Intel; Moore, of Moore’s law; and others—were intimately connected with Stanford University. As their firms grew, research and engineering talent was drawn from Stanford. The highly successful pairing of Stanford University and Silicon Valley established a model that other states sought to replicate. In the industry’s formative years, state funding was largely channeled to science and engineering schools [rather than semiconductor firms](#).

New York State was an early example.¹³ George Low, named president of Rensselaer Polytechnic Institute (located in Troy) in 1975, advocated partnerships between industry and universities, following the Stanford-Silicon Valley model. In 1981 he persuaded Governor Hugh Carey to provide \$30 million for the new Center for Industrial Innovation. More state funding followed. In 2003 the State University of New York at Albany partnered with Sematech to establish a semiconductor lab. Then, in 2008–09, GlobalFoundries, a private semiconductor firm, established two large fabs in upstate New York, directly employing almost 10,000 workers at high salaries. State subsidies to GlobalFoundries were quite modest. The real attraction was research and engineering talent [created by state funding](#).

Starting in the 1980s, other states followed the approach pioneered by California and New York. Georgia, Texas, Illinois, and Michigan were notable. State subsidies paid directly to chip companies were small compared to inducements for auto firms. Instead, like New York, states tried to replicate the Stanford-Silicon Valley model.

The CHIPS Act triggered a burst in state semiconductor subsidies paid directly to firms. Table 4 summarizes state subsidies offered or anticipated. The announced total, to be implemented over several years, appears to be around \$18 billion, with the lion’s share offered by New York. The Department of Commerce application for CHIPS Act funding does not absolutely require complementary state or local grants to qualify, but it requires a detailed description of such grants. Encouraged by corporate applicants, state governors responded accordingly. Without the CHIPS Act, direct state subsidies to semiconductor firms might be far smaller.

13 For the New York story, see the [CSIS report](#). [Industry clusters](#) contributed to the success.

Table 4

Recent US state semiconductor subsidies (millions of current US dollars)

State	Subsidies total ^a	Notes
Arizona	100.0	\$100 million investment from American Rescue Plan Act funding
California	40.0	More than \$40 million for two semiconductor companies
Colorado	1.5	2024–25 estimated general fund cost of \$1.5 million, more in later years
Florida	10.0	Approximately \$10 million
Idaho	n.a.	No fiscal or revenue note found
Illinois	n.a.	No fiscal or revenue note found
Kansas	304.0	No fiscal note found, but \$304 million has been awarded for a semiconductor investment
New York	15,500.0	Total tax credits capped at \$500 million per year for 20 years; \$5.5 billion reportedly already awarded
Ohio	650.0	Incentives could total up to \$650 million over 30 years
Oregon	24.8	Fiscal year 2025 estimated general fund cost of \$24.8 million
Pennsylvania	1,426.0	Authorized tax credits of up to \$141.6 million annually across a variety of investment types, with \$10 million allocated annually for semiconductor manufacturing
Texas	2.5	\$1.7 million through fiscal year 2025; approximately \$833,000 for fiscal years 2026–28
Total	18,058.8	
<i>Ratio to CHIPS Act budget (percent)</i>	23.2%	Ratio of US state subsidies total to the CHIPS Act budget of \$78 billion
<i>Ratio to US capex 2023 (percent)</i>	37.5%	Ratio of US state subsidies cumulated total to the capex of US semiconductor companies in 2023 of \$48.2 billion

n.a. = not available; capex = capital expenditures

a. Includes estimated costs, approved funding, and cash awarded. The period for state subsidies is roughly 2020–24.

Source: Tax Foundation, *States Enact Semiconductor Subsidies in the Wake of CHIPS* (<https://taxfoundation.org/blog/state-semiconductor-incentives>).

JAPAN

Japanese excursions into industrial policy began soon after World War II, reaching steel, shipbuilding, heavy machinery, chemicals, and much else. Akio Morita, the founder of Sony, led Japan into the semiconductor field through consumer products incorporating US chips, such as transistor radios and handheld calculators. In 1964, partnering with Sony to clear bureaucratic hurdles, Texas Instruments started making semiconductors in Japan.

In 1976 Japan launched the [Very Large-Scale Integrated Technology Research Project](#) (VLSI Project), which compelled cooperation between five large Japanese semiconductor firms: Fujitsu, Hitachi, Mitsubishi Electric, Nippon Electric, and Toshiba. The government contributed an initial subsidy of \$288 million to the VLSI Project (around \$72 million annually), and private firms contributed much more. Consequently, in 1977 public and private semiconductor R&D accounted for 26 percent of Japan's total R&D spending. Between 1976 and 1996 Japanese subsidies for R&D, including the VLSI Project, totaled [\\$571 million](#). Factors other

than the VLSI Project and kindred subsidies were probably more important to the subsequent success of Japan's semiconductor industry, notably low interest rates, which spurred heavy investment, a strong emphasis on product quality (meaning low chip defect rates), and [vertical integration](#) between chip producers and chip purchasers. According to Wolff, the US semiconductor industry saw joint research, sponsored by Nippon Telephone and Telegraph Corporation and the Ministry of Industry and Technology, as more important than subsidies.¹⁴ Vertical integration and joint research were Japanese industrial policy features never emulated in the United States.

The VLSI Project, which lasted until 1990, enabled Japanese dominance of the global DRAM market in the 1970s and 1980s.¹⁵ Unlike Europe, Japan generally [prohibited US firms](#) from establishing local production plants.¹⁶ Vertical ties between Japanese chip producers and commercial users ensured that imports occupied a small share of the local market. With the assurance of high prices in the domestic market, Japanese firms sold DRAMs at low prices in the world market. Thus, by 1989 Japan supplied [half](#) of the world chip market. While US firms, apart from Micron (financed by Jack Simplot, the Idaho potato baron) and Motorola, were exiting the DRAM market, 6 of the world's top 10 semiconductor firms by revenue were Japanese. Meanwhile, the Japanese firms Nikon and Canon were pushing the US firm GCA (once the sole producer) out of the lithography equipment market.

The year 1989 marked the [high point](#) of Japan's share of the world chip market. That same year Morita and Shintaro Ishihara published *The Japan That Can Say No*, a collection of essays critical of US tech firms. Between 1990 and 2020, two trends worked against the integrated Japanese chip firms. First was the separation between chip foundries and chip designers. The "pure-play" foundry firms, especially the Taiwan Semiconductor Manufacturing Company (TSMC), manufactured chips with fewer defects at lower prices than the integrated Japanese firms. And specialty design firms, such as Qualcomm and Broadcom, were better at their craft than integrated Japanese firms. The second adverse trend was the relative rise of new chips, such as microprocessors and application-specific integrated chips, and correspondingly the relative fall of DRAMs. Between 1990 and 2020 Japan's share of the world chip market steadily declined to just 10 percent, as did its technological prominence. In 2022 no Japanese companies ranked among the top 10 world chip firms by revenue.

As documented by the [Center for Strategic and International Studies \(CSIS\)](#), between 1990 and 2020 the Japanese government promoted collaborative projects between leading Japanese firms in hopes of reversing the decline, but these new initiatives were restrained compared to the VLSI Project. US trade policy during the George H.W. Bush, William Clinton, and Barack Obama presidencies frowned on foreign industrial policies that disadvantaged US firms.

14 Private communication from Alan Wolff.

15 *The Microelectronics Race*, a 1988 book authored by Howell et al., documents the prominence of the VLSI Project, and vertical *keiretsu* integration, in making Japan the leading DRAM manufacturer. Japanese technology was also first-rate for EPROM chips, but sales were small compared to DRAM chips. The VLSI collaboration led to electron beam lithography, a revolution in chip-making equipment technology, now dominated by the Dutch firm ASML.

16 According to Wolff (private communication), Fairchild tried to build a plant in Okinawa before the island reverted to Japanese control in 1972, but the project was rejected.

Owing to its dependence on US military protection, Japan paid close attention to US views. Two Japanese projects during this period were joint foundries: the Hinomaru Foundry in 2001 and the failed collaboration between Hitachi, Toshiba, and Renesas for an advanced foundry in 2005. Other projects entailed collaboration on chip design to create small, advanced semiconductors, such as the Asuka project for the 65 nm generation of semiconductors and the Millennium Research for Advanced Information Technology (MIRAI) project for the 45 nm generation.

None of these projects made much difference, but a new era dawned in 2020 as the US attitude toward industrial policy reversed from frown to smile. A 2023 paper published by CSIS tells the story. Japanese officials [cited the CHIPS Act](#) as justification for a massive resurgence of government measures. Taken together, Japan's post-2020 industrial policy actions far surpassed the VLSI Project. In 2021, Prime Minister Fumio Kishida's cabinet approved an umbrella budget of \$7.7 billion to revive Japan as a technological chip leader. The announced program, Japan's [Strategy for Semiconductors and the Digital Industry](#), aims to increase chip sales from \$30 billion in 2020 to \$112 billion in 2030. Additionally, [the strategy seeks](#) to at least maintain Japan's 10 percent share of the global market and develop logic and next-generation chips in cooperation with US firms. In November 2023 Japan committed an additional [\\$13.3 billion](#), split between manufacturing and R&D.

In August 2022, the same month Biden signed the CHIPS Act, [Japan sponsored Rapidus](#), a [bold partnership](#) to develop 2 nm chips. Rapidus connects 12 Japanese firms with IBM and Belgium's Interuniversity Microelectronics Center. In April 2023 [Japan provided](#) an initial subsidy of \$530 million and a subsequent subsidy of \$1.94 billion. When constructed, the Rapidus foundry is expected to cost \$35 billion, and Japanese government support is almost guaranteed.

Closely related to Rapidus is the Leading-edge Semiconductor Technology Center (LSTC) for advanced chips, bringing together Japanese firms and IBM with [\\$300 million](#) government support. The goal is to develop 1.4 nm chips within five years. LSTC is supported by Japan's existing public research organizations: the National Institute of Advanced Industrial Science and Technology, Riken (a scientific research institute largely funded by the government), and the University of Tokyo. LSTC is open to researchers from "like-minded" countries.

Rapidus and LSTC [are research arms](#) of Japan's industrial policy thrust. The manufacturing arms rely heavily on TSMC, the world's leading foundry firm that produces 70–90 percent of advanced chips. TSMC will build two new foundries in Kumamoto Prefecture. The first, announced in November 2021 and [operational](#) in February 2024, is a joint venture between TSMC, Sony, Denso, and Toyota; it received \$3.5 billion subsidies for a fab costing \$8.6 billion. The second, announced in February 2023, is a partnership between Sony and Denso to manufacture 5 nm and 10 nm chips in a foundry to be constructed by TSMC with a cost of \$7 billion and roughly \$2.3 billion subsidies. The first fab was constructed in two years, much faster than TSMC's experience with a new fab in Arizona. In addition to the two TSMC foundries, a subsidy of [\\$620 million](#) was announced for a partnership between Kioxia (Japan) and Western Digital (United States) to manufacture three-dimensional (3D) flash memory chips and [\\$1.3 billion](#) for Micron to expand its Hiroshima DRAM plant.

Japan's industrial policy exhibits three distinct features that contrast with the CHIPS Act. The features were nascent in the early VLSI Project and pronounced in the post-2020 surge. First, Japanese policy prominently emphasizes R&D. Second, it has narrowly defined targets: DRAM excellence in the VLSI episode and very small nanometer chips in the post-2020 surge. Third, it fosters, and even compels, cooperation between firms, both Japanese and foreign.

TAIWAN

In 1969 Texas Instruments opened a chip factory in Taiwan with the blessing of powerful economy minister K.T. Li. By the [early 1970s](#) Taiwan settled on semiconductors as a path to manufacturing success. The [Industrial Technology Research Institute](#) (ITRI) was founded with modest public funding in 1973 and contracted with the Radio Corporation of America to develop ICs. Until the 1980s, however, Taiwan's engagement in the semiconductor industry was limited to ATP. ITRI then became the launching pad for Taiwan's [two most successful](#) semiconductor firms: the United Microelectronics Corporation (UMC) in 1980 and TSMC in 1987. Both firms started life with government funds; for TSMC, a launch figure of [\\$200 million](#) is reported, [half from government sources](#). Additionally, they were given space in [Hsinchu Science Park](#), created by the government in 1980 and modeled after Silicon Valley. Other semiconductor firms were invited to the science park. Apart from these subsidies, Taiwan's incentives for the industry are not reported on English websites. Another benefit, but technically not a subsidy, is Taiwan's low corporate tax rate, now 20 percent.

While early government support was critical for Taiwan's stunning success in semiconductor production, two other factors were equally essential. First was [Taiwan's recruitment](#), at the insistence of Li, of Dr. Morris Chang to lead ITRI in 1985 and create a semiconductor industry. Chang, born in China, proved as central for Taiwan as Robert Noyce did for the United States. Chang was educated at Harvard, the Massachusetts Institute of Technology, and Stanford, and he had worked on semiconductors for 25 years at Texas Instruments before moving to Taiwan. In 1987, from his perch as president and chairman of ITRI, [Chang launched TSMC](#) in collaboration with Philips, the Dutch electronics firm, and with public and private financial support.

A second essential factor was Chang's decision to [adopt the business model](#) pioneered by UMC: produce chips [on a contract basis](#) for other companies—what came to be called a pure-play foundry. This was a sharp departure from integrated firms that both designed and manufactured chips. Li insisted that TSMC partner with an integrated firm, but both Texas Instruments and Intel were skeptical of the pure-play foundry and turned down the offer. Instead, Philips was persuaded to transfer its technology and put up \$58 million for a 27.5 percent share of TSMC. As a contract manufacturer, TSMC's profit margin per chip was small, but it more than made up on volume what it lost on price. An attractive TSMC feature was its ability to supplement chip designs brought by clients with its own intellectual property blocks—namely, pieces of chip logic purchased from independent vendors. Over time TSMC has reduced the nanometer dimensions of a chip: It will soon produce 2 nm chips and is seeking 1.4 nm chips within a few years.

Today TSMC operates more than 15 foundries in China, Germany, Japan, Taiwan, and the United States, and it manufactures a [dominant share](#) of the world's advanced chips. In 1997 Micron brought an [antidumping case](#) against TSMC, and Taiwan retaliated with an [antidumping case](#) against Micron. The cases were eventually settled. The Congressional Research Service reports that [90 percent](#) of global leading-edge chip production is concentrated in Taiwan. TSMC customers include most US chip firms, including Nvidia; several from China, including Huawei;¹⁷ and many based in other jurisdictions. In 2022 Taiwan as a whole produced 64 percent of the world's semiconductors and commanded 70 percent of the global production capacity below 7 nm. Including TSMC, the Taiwan semiconductor industry had over [300,000 employees](#) in 2022. In addition to its [geopolitical significance](#), the industry is critical to Taiwan's economy. For that reason, the US CHIPS and Science Act, passed in August 2022, set off alarms in Taipei.

In response, Taiwan's legislature enacted [new R&D incentives](#) in January 2023. The Chip-based Industrial Innovation Program was passed in [November 2023](#), providing [\\$9.2 billion](#) funding in 2024. Standard provisions include a [25 percent tax deduction](#) for R&D outlays and a 5 percent tax credit for about \$300 million spent on new equipment for [advanced process technology](#). The Ministry of Education has bolstered the country's training programs. Also, block subsidies are available on a discretionary basis for individual firms. Together, Nvidia and Micron will receive \$375 million. ASML will spend \$157 million to build a plant in Taiwan, but [public funding](#) was not announced.

SOUTH KOREA

As early as the 1960s, the South Korean government took an interest in semiconductors, but public support was confined to research on a small scale. According to a knowledgeable observer, the research institute brought together experts from major firms and university professors. Together, they operated as a task force to spur the Korean semiconductor industry.¹⁸ The government also attempted to recruit US firms. While the government opposed the establishment of majority-owned foreign firms in Korea, an exception was made for Fairchild, which invested \$2.3 million with 100 percent ownership in 1969. Its operations were, however, [limited to ATP](#). Between 1967 and 1971, a few other foreign firms were [approved for entry](#) with 100 percent ownership, including Motorola.

The Ministry of Trade issued its [Eight-Year Plan](#) for Electronics Industry Promotion in 1969, which stressed technical education and exports. The plan also provided a \$50 million promotion fund. In that same year, the Samsung *chaebol* entered the electronics industry. Because Samsung's entry was opposed by [59 smaller Korean electronics firms](#), the ministry restricted the range of products Samsung could make and required that all production be exported. The restrictions were dropped [in 1971](#).

17 In November 2024 TSMC [announced](#) that it would no longer produce advanced chips for Chinese firms.

18 Observation by Han-Koo Yeo, Korean trade minister (2021–22). Also see a [summary](#) of Korea's success in the DRAM industry.

Within a few years, three *chaebol* firms—Samsung, Goldstar, and Hyundai Electronics—dominated the Korean semiconductor industry. These firms enjoyed implicit benefits [from their *chaebol* status](#): preferential access to domestic bank credit, an undervalued exchange rate, and the financial strength to fund startup semiconductor operations. However, apart from the small promotion fund and infrastructure in the Gumi National Industrial Complex (opened in 1970), explicit government support [was slight](#).

During the heavy and chemical industry phase of Korean industrial policy (1973–79), electronics were named as an industry [deserving support](#). However, because consumer electronic exports were booming, the *chaebols* received [little or no direct subsidies](#) for their chip operations.

Despite tepid public support in the 1970s, 1980s, and 1990s, Samsung, Goldstar, and Hyundai Electronics became export powerhouses, [first for consumer electronics](#), then for chips (Goldstar and Hyundai Electronics merged to become SK Hynix). According to Miller (*Chip War*), in February 1983 Lee Byung-Chul, the formidable leader of Samsung, reached the fateful decision to manufacture chips. A contemporary and knowledgeable observer, B.M. Byun, cites [five factors](#) for the stunning chip success of Samsung and other *chaebol*: bold investment, despite occasional heavy losses; concentration in memory devices (DRAM, static random access memory [SRAM], read-only memory [ROM]); research outposts in Silicon Valley with investments totaling \$1 billion and multiple technology licenses from US and Japanese firms; highly qualified Korean scientists and engineers; and government support for R&D and manpower training.

The main R&D support in the mid-1990s was a \$500 million, five-year R&D program (Electro-21), managed by the Electronics and Telecommunications Research Institute, and a \$150 million fund for facility investments. Apart from these subsidies, the government confined its role to indicative planning in the 1990s. Success in the 1980s and 1990s mainly was due to *chaebol* initiatives and Korean science, technology, engineering, and mathematics education. In addition to booming exports, a technical indicator of *chaebol* proficiency was the exponential rise of Samsung’s memory chips from 64K DRAMs in 1984, based on technology licensed from Micron, to [256K DRAMs](#) in 1995, based on in-house technology.

By the early 1990s Korea had become such a successful exporter that the United States pressured its ally to liberalize import barriers and revalue the exchange rate. Micron, a leading DRAM producer, brought an [antidumping case](#) in 1992. The Department of Commerce determined that DRAMs were indeed being dumped, but [at low margins](#): Samsung, 0.74 percent; Goldstar, 4.97 percent; and Hyundai Electronics, 7.19 percent.

Today Korea produces over [40 percent](#) of world DRAMs, around 8 percent of sub-10 nm chips, and around \$100 billion in chips annually. Owing to *chaebol* successes, which became apparent in the 1990s, the Korean government had no reason to subsidize the industry until SIA started promoting what became the CHIPS Act, following Biden’s election in 2020.

In response, President Moon Jae-in (2017–22) launched a subsidy strategy with three central elements: a new cluster of semiconductor fabs would rise in the so-called K Semiconductor Belt at Yongin, removed from the Seoul environs; tax credits would be awarded for new construction at 10–20 percent rates and

for R&D at 40–50 percent rates; and substantial cash subsidies would be paid to foreign firms bringing high technology, [50 percent](#) of cost in the Seoul area and 80 percent of cost outside. Before leaving office, Moon also passed the [National High-Tech Strategic Industry Act](#), tailored to the semiconductor industry, which enabled additional tax deductions and R&D support on a discretionary basis.

[One estimate](#) places the cost of tax credits enacted by President Moon and his successor, President Yoon Suk Yeol, at \$55 billion to \$65 billion.

In 2022 newly-elected President Yoon, seen as more partial to the *chaebols* than his predecessor, went further. He sponsored the [Korean Chips Act](#), raising [tax credits](#) from 8 percent to 25 percent for plant investment by *chaebol* firms. For the year 2023, firms were given [an extra 10 percent credit](#) for investments during the preceding three years. At the Yongin site for the new semiconductor “[megacluster](#),” SK Hynix is projected to invest \$91 billion, and Samsung Electronics is projected to invest \$220 billion. Early in 2023, a leading Samsung executive saw Korea in a “[chip war](#)” with the United States. The Korean Chips Act ensured that Korean tax credit rates are more generous than Japan, Taiwan, or the United States. Moreover, Korea is offering [generous cash grants](#) to foreign chip firms that build plants in Korea. Among other foreign firms, the leading equipment maker, ASML, will [establish a plant](#) in Korea. The Ministry of Trade, Industry and Energy will spend approximately [\\$900 million](#) to develop AI chip technology by 2026.

As a result of these incentives, Korean officials [predict](#) that the chip industry will invest at home [\\$450 billion](#) between 2021 and 2030, and that chip exports [will double](#) from \$100 billion in 2020 to \$200 billion in 2030. While Samsung and SK Hynix have received [subsidies for US fabs](#) from the CHIPS Act, and despite [cordial conversations](#) between US and Korean officials, in early 2023 Korea [criticized](#) the detailed obligations [required to receive](#) US funds. Differences were resolved, and in April 2024 Samsung received preliminary terms for a large grant under the CHIPS Act for plants in Texas. SK Hynix received preliminary terms for its Indiana plant in August 2024.

CHINA

China’s semiconductor story is a [long saga](#) of [industrial policy](#), characterized by rising subsidies and punctuated by disappointments. The story began in 1956 with the production of transistors in a state lab and, more importantly, a State Council decision to make semiconductors a national priority with degree programs in five leading universities. Soon after, in 1960, several Chinese firms initiated industrial training, most prominently state-owned Huajing Group’s Wuxi Factory No. 742. Meanwhile, starting in 1963, Fairchild, Texas Instruments, and other US firms opened ATP plants in Hong Kong, attracted by cheap labor.

In 1965 the Chinese Academy of Sciences began research on ICs and, at the time, was ahead of Korea and Taiwan. During this phase, which lasted until 1980, the industry was split between research in universities and state labs and manufacturing activity carried out by some 40 factories.

Deng Xiaoping came to power in 1978, following Mao Tse-tung’s death. Soon after, the Sixth Five Year Plan (FYP) (1981–85), created the Computer and Large-Scale IC Lead Group with the goal of modernizing the industry. The government spent RMB 1.3 billion (roughly \$650 million at the prevailing exchange rate, then

about RMB2 to \$1) during the Sixth FYP, importing 24 secondhand manufacturing lines. Some 30 poorly performing Chinese firms were pared down to 5 “key” firms. Nevertheless, an American researcher visiting Shanghai in the mid-1980s found the production to be 10–15 years out of date, with defect-free yields under 40 percent.

In the 1990s, both the Eighth FYP (1991–95) and the Ninth FYP (1996–2000) featured fresh semiconductor subsidies while further narrowing the list of favored Chinese firms and mandating joint ventures with foreign firms. The industry was concentrated in the Yangtze Delta, notably in Shanghai, Suzhou, and Wuxi. Under the Eighth FYP, Project 908 awarded Wuxi Factory No. 742 a subsidy of RMB2 billion (then about \$240 million at the prevailing exchange rate, RMB8.35 to \$1) and formed a joint partnership with Lucent. However, production was slow to reach the market. The Ninth FYP featured Project 909, with a joint venture between Shanghai Huahong and Nippon Electric (Japan) to produce DRAMs. Unfortunately, the 2002 DRAM recession led to massive losses, and the partnership was restructured.

The year 2002 saw the founding of the Semiconductor Manufacturing International Corporation (SMIC) in Shanghai led by Zhang Rujing (also known as Richard Chang). Zhang, a Texas Instruments and TSMC chip veteran, was born in China, raised in Taiwan, and educated in the United States. He brought hundreds of Taiwanese engineers to launch SMIC. Half the initial capital came from foreign investors. But eventually SMIC became a state-owned enterprise; by 2015 the chairman was a former official of the Ministry of Industry and Information. The Tenth FYP (2001–05) provided RMB380 billion (about \$47 billion) of semiconductor subsidies plus tax preferences, with SMIC as the major beneficiary. SMIC enjoyed a five-year tax holiday, followed by five years of taxation at half the normal rate, plus tariff exemptions, reduced value-added tax, and loans from state banks. SMIC sustained its technical proficiency by recruiting engineers from Singapore, Taiwan, and the United States; today SMIC is the leading Chinese chip manufacturer and one of the world’s largest foundries. Facing losses after 2005, SMIC received an additional \$2.3 billion in central and municipal subsidies. In 2009 SMIC lost a suit for technology theft filed by TSMC and had to pay \$200 million.

Leading Taiwanese and Korean firms also located subsidiaries in Suzhou before and during the 10th FYP. The firms included Samsung, UMC (Taiwan), Hitachi and Mitsubishi (Japan), and Advanced Micro Devices (AMD; United States). Leading Japanese and Korean firms favored Wuxi. The large indigenous firm China Steel Machinery Corporation (CSMC) focused on standard chips. By 2007 chip firms located in the Yangtze Delta employed 750,000 workers and exported chips worth \$50 billion. Subsidiaries of foreign firms were largely responsible for production and exports during the 10th and 11th FYPs. In response, the central government rhetorically emphasized indigenous innovation.

In 2014 China issued *Guidelines to Promote National Integrated Circuit Industry* (the National IC Plan), calling for central and provincial funding of \$150 billion to bolster the semiconductor sector with inbound and outbound foreign direct investment designed to keep pace with new technology and to mass-produce chips at or smaller than 16 nm/14 nm by 2020. The three phases of the National IC Plan (2014, 2019, and 2023) were estimated to raise roughly

\$92 billion from the Ministry of Finance and state-owned companies. Provincial and municipal governments are expected to contribute another [\\$50 billion](#).

In 2015 Chinese leaders launched [Made in China 2025](#), a plan to make the country dominant in key manufacturing sectors, including the semiconductor industry. The announced goal was [70 percent](#) self-sufficiency by 2025. Together, the National IC Plan and the Made in China 2025 essentially guaranteed a steady flow of state subsidies for the next decade and a concerted effort to acquire Western technology. Prior to 2014, total Chinese mergers and acquisitions (M&A) deals with US firms amounted to under \$220 million; by 2017, deals worth \$11 billion had been announced. IBM, Qualcomm, and AMD all made deals in China, welcomed by China's security apparatus. Access to the Chinese consumer electronics market was a significant incentive. Similar deals were concluded by European firms, including Arm Holdings, the UK chip designer.

Finance for the M&A spree largely came from [state sources](#). One channel was Tsinghua Unigroup, an offshoot of Tsinghua University that mixed public and private funding for chip ventures. In 2017 Tsinghua Unigroup received \$17 billion from China Development Bank and \$7 billion from the China Integrated Circuit Industry Investment Fund, both controlled by the state. Zhao Weiguo, a billionaire tycoon and stakeholder in Tsinghua Unigroup, went so far as to float a [\\$23 billion offer](#) for Micron in 2015. While that offer was rebuffed (later, Micron [suffered from](#) Chinese technology appropriation),¹⁹ between 2014 and 2018 nearly all major US chip firms entered into joint ventures with Chinese partners, accompanied by ensuing pressure to transfer technology. However, China's attempt to invest in a small US chip firm, Lattice Semiconductors, was [blocked](#) by then President Donald Trump. The State Council [announced](#) in 2020 that corporate income taxes on the earnings of advanced fabs would be waived for 10 years.

The Congressional Research Service reports that cumulative public support for the Chinese semiconductor industry reached [\\$322 billion](#) as of 2023. A recent survey of national industrial policies, authored by Dr. Chen-Yuan Tung, a Taiwanese diplomat, provides current subsidies to leading Chinese chip firms, as shown in table 5.

Despite its robust industrial policy, China remains [a major importer](#) of chips for its huge consumer electronics and automotive industries and seems some distance from self-sufficiency either in semiconductor quantity or quality.

EUROPEAN UNION

In April 2021 Intel's chief executive officer (CEO), Patrick Gelsinger, claimed that Europe's share of world chip production fell from 44 percent in 1990 to 10 percent in 2020. That statistic, picked up by Bloomberg, fueled Europe's subsidy surge. The figures originated in Exhibit 2 of the influential [BCG and SIA report](#) that inspired the CHIPS Act. However, as Jan-Peter Kleinhans [has shown](#), Exhibit 2 is misleading because it omits semiconductor wafers smaller than 8 inches (200 mm). A more accurate statement, including smaller wafers, is that in 1990 Europe had 10.1 percent of world fab capacity, and in 2020 it had 9.4 percent. Not a stellar showing, but not a collapse. Nevertheless, the claimed

19 In 2023 Micron was [blocked](#) from selling to Chinese companies following a review by China's Cyberspace Administration.

Table 5

China's top 10 chip subsidy recipients (millions of current US dollars)

Company	Subsidies received in	
	2022	2021
Semiconductor Manufacturing International Corporation	274	341
Sanan Optoelectronics	144	129
Tianshui Huatian Technology	65	71
Wingtech Technology	54	49
HC SemiTek	46	59
Naura Technology	45	43
Anhui Truchum	42	31
Cambrian Technologies	38	31
ChaoZhou Three-Circle	30	19
Loongson Technology	27	11
Total	766	787

Note: Numbers may not add up due to rounding.

Source: Chen-Yuan Tung, *Taiwan and the Global Semiconductor Supply Chain* (<https://www.roc-taiwan.org/uploads/sites/86/2023/08/20230824-TAIWAN-AND-THE-GLOBAL-SEMICONDUCTOR-SUPPLY-CHAIN.pdf>).

decline of the EU production share stuck in the official European mind, with important industrial policy consequences.

In the 1950s European chip producers, such as Siemens, Philips, and Thomson-CSF largely sold their wares to consumer and industrial firms. In the 1960s European firms were far behind IBM when the computer revolution swept advanced countries. In turn, European chip firms trailed their US competitors in manufacturing ICs. In the 1970s Europe concentrated its industrial policy on [matching IBM computers](#) rather than on semiconductors.

For decades, [Europe's semiconductor industrial policy](#) was centered on a 17 percent tariff (eliminated in 2021), coupled with mandated government procurement (particularly by Britain and France), and support for national champions. In Kenneth Flamm's judgment,²⁰ this phase of industrial policy ended in failure. European chip firms continued to produce a high proportion of discrete transistors and diodes rather than the rapidly growing volume of ICs made by US and Japanese firms. Consequently, the share of European firms in world chip production declined from about 25 percent in 1975 to around 12 percent in 1985.

Meanwhile, US chip firms set up ATP subsidiaries in Europe to skirt the high European tariff. Moreover, Flamm calculates that 20-30 percent of European chip imports benefited from duty suspensions in 1988. Unlike Japan, Europe welcomed tariff-jumping plants established by US chip firms. As early as 1974,

20 Kenneth Flamm, "Semiconductors," chapter 5 in *Europe 1992: An American Perspective*, ed. Gary Clyde Hufbauer (Washington: Brookings Institution, 1990).

18 affiliates of foreign firms were manufacturing or assembling chips in Europe. Contemporary observers claimed that the welcome mat for foreign firms led to [anemic performance](#) by European producers.

The 1980s brought [a fresh burst](#) of European semiconductor industrial policy, [emphasizing R&D](#). In 1983 Netherlands and Germany paid a third of the billion-dollar cost for a joint Philips-Siemens semiconductor plant (the “[Megaproject](#)”). Later this became part of the European Eureka project, sponsored by President François Mitterrand of France in response to President Reagan’s Strategic Defense Initiative.

In 1984 the European Community (EC) established the [European Strategic Program for Research and Development in Information Technology](#) (Esprit) for a cost of about [\\$900 million](#), half paid by the EC and [half by firms](#), to [support chip research](#) and other projects. In 1987 a second-stage Esprit was announced with a budget of about \$2 billion. In 1989, responding to the US Sematech venture, the EC created the [Joint European Submicron Silicon Initiative](#), with a budget of about [\\$2.4 billion](#) over eight years.

World semiconductor prices softened in 1984, prompting the United States-Japan STA in 1986. The STA [covered chip prices](#) not only in the United States and Japan but also in third-country markets, thereby inaugurating an era of managed trade, [much to the consternation](#) of European officials.²¹ They saw the STA as a surprising turn of US policy away from free trade, with adverse effects on European chip producers and consumers. Over the next few years, Europe reconfigured its own chip trade policies and brought a successful General Agreement on Tariffs and Trade case against the STA. Europe also brought a dumping case against Japanese DRAMs in 1989 and concluded the case with a Europe-Japan price-fixing agreement.

During the first two decades of the 21st century, not much happened on the European semiconductor policy front. The European Commission did approve [\\$11 billion](#) for R&D and called for a multipronged approach to raise the European share of global chip production to 20 percent by 2020. The results were disappointing. While the EU chip industry lagged its competitors, the decline as a share of world production was not as large as Intel CEO Gelsinger claimed. Nevertheless, in 2021 EU firms made [very few](#) advanced chips. From a technology perspective, the leading EU firm was [not a mainline foundry](#) but rather the Dutch manufacturer of chip-making equipment, [ASML](#).

As in the US debate over the CHIPS Act, the EU debate over the European Chips Act was heavily influenced by the economic [cost of chip shortages](#) during the COVID pandemic. In 2021, spurred by the proposed CHIPS Act and Asian dominance of advanced chips, European Commission President Ursula von der Leyen [called for](#) Europe to plunge into the industrial policy race. The commission soon published a detailed [staff paper](#) that documented the relative decline of European chip revenue and capex.

The European Union’s Digital Compass 2030, issued in 2021, announced the ambitious goal to [increase Europe’s share](#) of world chip production from [10 percent to 20 percent](#) by 2030. Eventually this led to the [Chips for Europe](#)

21 To be fair, the era of management started with the Japanese VLSI Project, which combined a closed home market with joint research and subsidization.

Initiative setting goals and the [European Chips Act](#) providing money in September 2023.

The [European Chips Act](#), with a public and private budget of [\\$47 billion](#), [aspired to fulfill](#) von der Leyen's goal of [doubling the European share](#) of global chip production from 10 percent to [20 percent](#) by 2030. The Chips Joint Undertaking (Chips JU) became the leading program under the Chips for Europe Initiative, which in turn is the main component of the European Chips Act. Chips JU began funding projects in [November 2023](#). The projected public budget through 2030 for the Chips for Europe Initiative is about \$17 billion, of which about \$12 billion is allocated to Chips JU. Among other goals, Chips JU will support research into quantum chips and 2 nm advanced chips. Most European Chips Act funds are provided by [member state governments](#) (allowed a pass from EU state aid rules), leading to a concentration in Germany and France. These countries have [encouraged projects](#) by Intel (\$10.9 billion from Germany), Infineon Technologies (\$5 billion from Germany), and a joint venture between STMicroelectronics and GlobalFoundries (\$3.1 billion from France).

Andrew Johnston and Robert Huggins provide a [good survey](#) of the current chip industry in Europe. With very modest subsidies, the Dutch firm ASML, a 1984 spinoff from Philips, became the world's [foremost producer](#) of lithography equipment. By market capitalization, the [top six European producers](#) are ASML, Arm Holdings (UK design firm), NXP Semiconductors (Dutch spinoff from Philips in 2005), Infineon (German), STMicroelectronics (Swiss), and Ams (Austrian). Some firms have recently received cash grants, and historically they most benefited from high tariffs, government procurement, and the erstwhile market agreements with Japan.

While welcoming the European Chips Act, independent scholars suggest that it is [too small](#) to achieve its ambitious goals and that more emphasis should be placed on scaling up regional semiconductor clusters.

COMPARATIVE DATA ON JURISDICTION SUBSIDIES

Four different sets of data enable rough cross-country comparisons of semiconductor subsidies. One set is based on the OECD report covering the period 2014–18. The second set is based on reported cash subsidies during the period 2020–24. The third set is based on the total cost of ownership (TCO) of a foundry as calculated by BCG and SIA. The fourth set is based on a recent National Bureau of Economic Research (NBER) working paper. Supplementing these four sets of subsidy data are corporate tax rates for firms headquartered in different countries.

OECD Subsidy Report, 2014–18

In 2019 the OECD published a careful and detailed analysis of subsidies received by 21 leading semiconductor firms, headquartered in different countries, during the years 2014–18. This is the best existing dataset of comparative firm subsidies.²² Because the 21 leading firms do not cover the entire industry, table 6 understates the total dollar volume of subsidies. The OECD should now update the analysis as a public service.

22 But Martin Chorzempa faults the OECD analysis for not identifying Chinese subsidies to Korean firms and more generally for understating Chinese subsidies.

Table 6
Subsidies from all governments by headquarter jurisdiction, 2014–18 (billions of current US dollars)

<i>a. All firms</i>										
Item	Switzerland	China	Germany	Japan	Korea	Netherlands	Taiwan	United States	Total	Total
Total revenue	39.3	64.6	36.6	270.0	1,091.4	39.9	222.5	646.9	2,411.0	2,411.0
Budgetary support	1.7	2.6	0.7	0.6	8.8	1.2	5.1	15.2	35.9	35.9
Total financial subsidies	2.4	16.6	0.2	29.4	2.7	1.0	6.9	12.3	71.4	71.4
Total support	4.1	19.1	0.8	30.0	11.6	2.2	12.1	27.4	107.3	107.3
Budgetary support (percent of revenue)	4.29	3.98	1.79	0.21	0.81	3.09	2.31	2.35	1.49	1.49
Other financial subsidies (percent of revenue)	6.06	25.66	0.48	10.90	0.25	2.46	3.11	1.89	2.96	2.96
Total support (percent of revenue)	10.36	29.64	2.27	11.11	1.06	5.55	5.42	4.24	4.45	4.45
<i>b. Only private-invested firms</i>										
Item	Switzerland	China	Germany	Japan	Korea	Netherlands	Taiwan	United States	Total	Total
Total revenue	—	—	36.6	237.2	1,091.4	39.9	218.4	646.9	2,270.4	2,270.4
Budgetary support	—	—	0.7	0.4	8.8	1.2	5.1	15.2	31.4	31.4
Total financial subsidies	—	—	0.2	28.7	2.7	1.0	6.9	12.3	51.8	51.8
Total support	—	—	0.8	29.2	11.6	2.2	12.0	27.4	83.2	83.2
Budgetary support (percent of revenue)	—	—	1.79	0.19	0.81	3.09	2.33	2.35	1.38	1.38
Other financial subsidies (percent of revenue)	—	—	0.48	12.11	0.25	2.46	3.17	1.89	2.28	2.28
Total support (percent of revenue)	—	—	2.27	12.30	1.06	5.55	5.50	4.24	3.67	3.67

c. Only government-invested firms

Item	Switzerland	China	Germany	Japan	Korea	Netherlands	Taiwan	United States	Total
Total revenue	39.3	64.6	—	32.7	—	—	4.1	—	140.7
Budgetary support	1.7	2.6	—	0.1	—	—	0.0	—	4.4
Total financial subsidies	2.4	16.6	—	0.7	—	—	0.0	—	19.6
Total support	4.1	19.1	—	0.8	—	—	0.0	—	24.1
Budgetary support (percent of revenue)	4.29	3.98	—	0.40	—	—	1.01	—	3.15
Other financial subsidies (percent of revenue)	6.06	25.66	—	2.15	—	—	—	—	13.97
Total support (percent of revenue)	10.36	29.64	—	2.55	—	—	1.01	—	17.12

— = none

Notes: Calculated based on the 2019 Organization for Economic Cooperation and Development (OECD) report that covers 21 firms over 2014–18 (see supplement table). Other financial subsidies and total support are based on high estimates in the OECD report. Dashes mean no private-invested or government-invested firms in the respective countries.

Source: OECD, *Measuring Distortions in International Markets: The Semiconductor Value Chain*, OECD Trade Policy Paper 234 (<https://doi.org/10.1787/8fe4491d-en>).

Supplement to table 6

List of firms by country covered in OECD (2019) report

Country	Company	Category
China	Shanghai Huahong	State
	Jiangsu Changjiang Electronics Technology	State
	Semiconductor Manufacturing International Corporation	State
	Tsinghua Unigroup	State
Germany	Infineon Technologies	Private
Japan	Renesas	State
	Toshibaa	Private
Korea	Samsung Electronics	Private
	SK Hynix	Private
Netherlands	NXP Semiconductors	Private
United States	Amkor Technology	Private
	Intel	Private
	Micron	Private
	Nvidia	Private
	Qualcomm	Private
Taiwan	Texas Instruments	Private
	Advanced Semiconductor Engineering	Private
	Taiwan Semiconductor Manufacturing Company	Private
	United Microelectronics Corporation	Private
	Vanguard Semiconductor	State

a. Toshiba data are for 2013-17.

Table 6 reorganizes the OECD data by headquarters country. Since major chip firms produce in several countries, their foreign subsidiaries often receive subsidies from host countries. In fact, during the period 2014-18, most subsidies to US-headquartered firms came from countries other than the United States. Nevertheless, table 6 attributes all subsidies to the headquarters country because, in competition between countries, the location of headquarters matters. To be sure, the CHIPS Act seeks to boost chip manufacturing on US territory, whether by US- or Asian-headquartered firms—not to boost the dominant US-headquartered firms such as Intel, Micron, or Nvidia. But taking a longer view of global competition, the relative strength of US-headquartered firms certainly matters to advocates of industrial policy.²³

23 Strident political opposition to Nippon Steel's proposed acquisition of US Steel illustrates the importance attached to corporate headquarters. Nippon Steel would bring advanced technology and new investment to US Steel, but those benefits are overshadowed in political debate by the shift of headquarters from the United States to Japan.

Looking first at totals in panel a, direct budget support (cash and tax credits) amounted to \$36 billion for the 21 firms. Support was provided not only by the home country but also by host countries. Financial support through low-interest loans and equity financing (again from all sources) was almost twice as large, amounting to \$71 billion of subsidies for the 21 firms. Total support over the period reached \$107 billion, about \$21 billion a year for five years.

Dollar amounts were largest for firms headquartered in the biggest economies—the United States (\$27 billion) and Japan (\$30 billion)—but a more interesting finding is the wide range of subsidies expressed as a percentage of firm revenues. Chinese firms hit the jackpot, with subsidies equivalent to almost 30 percent of revenue. Next largest were Swiss and Japanese firms, 10 percent and 11 percent, respectively. Netherlands, Taiwan, and the United States were down in the 4–5 percent range. Least favored were German and Korean firms, at 1–2 percent.

Panels b and c distinguish between private- and government-invested firms. Not surprising, government-invested Swiss and Chinese firms top the charts in terms of subsidies expressed as a percentage of revenues. More surprising is that Japanese and Taiwanese government-invested firms fared worse than their private-invested competitors.

Cash Grants, 2020–24

With limited resources, it was not possible for this report to update the detailed OECD semiconductor subsidy report covering the years 2014–18. The OECD report covers the total range of subsidies received by 21 major chip firms: direct grants, tax credits, concessional loans, and equity infusions. Drawing on official documents and news reports, we compiled table 7, which provides a sample of direct grants either disbursed during the years 2020–24 or enacted during the period. Many of the enacted grants (such as CHIPS Act grants) will be disbursed after 2024.

Panel a of table 7 attributes direct grants to the headquarters economy of recipient firms. Most grants are, of course, given to locally based recipient firms for projects in the home country. However, in panel a, a grant, for example, to TSMC for a fab in Japan would be attributed to Taiwan. The disbursed total of such grants for the Big 6 semiconductor jurisdictions for the years 2020–24 amounted to \$59 billion. By comparison, the OECD calculated budgetary support (i.e., direct grants and tax credits) of \$36 billion to 21 firms for the years 2014–18.

Evidently, subsidy competition—just in the form of direct grants—became much more intense as the years passed. In the years 2020–24, TSMC and a few other Taiwan-headquartered firms were the largest recipients of direct grants, some \$22 billion. They were followed by US-headquartered recipients with \$16 billion.

Panel b of table 7 summarizes direct grants for projects launched in each of the Big 6 semiconductor jurisdictions, whether initiated by home firms or foreign firms. In terms of disbursed grants during the 2020–24 years, US projects were the leader with \$24 billion, followed by Japan with \$16 billion. Calculated this way, the Big 6 disbursed grants during the years 2020–24 totaling \$56 billion.

Panel b of table 7 also reports grants enacted by each of the Big 6 jurisdictions between 2020 and 2024, whether or not the funds were disbursed.

Table 7

Sample of cash grants, 2020–24 (billions of current US dollars)

<i>a. Disbursed grants by the headquarters economies of recipient firms annually^a</i>								
Headquarters economy	2020	2021	2022	2023	2024	Disbursed total		
China	1.5	1.8	1.8	1.8	1.8	8.6		
European Union	—	—	—	—	—	—		
Japan	—	—	2.2	—	4.4	6.6		
Korea	—	—	—	—	6.0	6.0		
Taiwan	—	—	3.5	7.1	11.5	22.1		
United States	—	—	—	2.2	13.9	16.0		
Total	1.5	1.8	7.4	11.1	37.5	59.3		
<i>b. Sample of disbursed and enacted grants by donor economies annually^b</i>								
Donor economy	2020	2021	2022	2023	2024	Disbursed total	Enacted total	Combined total
China	1.5	1.8	1.8	3.3	1.8	10.1	40.0	48.3
European Union	—	—	—	6.6	—	6.6	69.2	75.7
Japan	—	—	5.7	0.2	9.7	15.6	13.0	18.9
Korea	—	—	—	—	—	—	—	—
Taiwan	—	—	—	—	—	—	—	—
United States	—	—	—	1.0	22.8	23.8	52.7	53.4
Total	1.5	1.8	7.4	11.1	34.3	56.1	174.9	196.4

— = none

a. The “headquarters economies of recipient firms” means that the \$6.6 billion grant to the Taiwan Semiconductor Manufacturing Company (TSMC) from the US government for the Arizona fabs are attributed to Taiwan in panel a.

b. The “donor economy” means that the \$6.6 billion grant to TSMC from the US government for the Arizona Fabs are attributed to the United States in panel b.

Notes: Panels a and b differ in total disbursed grants because some grants cannot be traced to specific governments based on company financial reports, or the grants are given by economies other than the Big 6. The disbursed date is defined as either an explicit disbursement date or the report date of grants awarded. The European Union includes the European Union and its member states (mainly Germany). The grants received by Chinese companies in 2021, 2023, and 2024 are estimated based on grants in 2020 and 2022. The final column shows the total amount of grants disbursed and enacted from 2020 to 2024 without double counting. We assume China, the European Union (including Germany), and Japan used the enacted grants to disburse grants in 2024, while disbursed grants from 2020 to 2023 are additional to the enacted grants. The combined total of US grants includes CHIPS Act grants and \$723 million grants from the Ohio state government to Intel.

Source: News reports, research reports, and company financial statements no later than April 9, 2024.

The enacted total for all six jurisdictions amounts to \$175 billion, most to be disbursed later in the 2020 decade. The combined total of disbursed and enacted direct grants (without double counting) between 2020 and 2024 for all Big 6 jurisdictions comes to \$196 billion.

To summarize, direct grants to the chips industry surged in the early 2020s. While comparable data could not be found for other subsidies, the experience documented by the OECD between 2014 and 2018 suggests that the grant-equivalent benefit of concessional loans, equity infusions, and tax credits collectively exceed—by a substantial amount—the magnitude of direct grants.

Table 8

Subsidies for semiconductor fabs (percent reduction of total cost of ownership)

Reduction type		United States	Japan	Korea	Taiwan	China	Germany
Capital expenditures	Land	50	75	100	50	100	100
	Construction and facilities	10	10	45	45	65	35
	Equipment	6	10	20	25	35	5
Operating expenditures	Labor and benefits	5	5	5	5	33	7
Tax	Corporate tax	n.a.	n.a.	60	n.a.	75	n.a.
	State tax	100	n.a.	n.a.	n.a.	n.a.	n.a.
	Property tax	100	100	100	n.a.	n.a.	n.a.
Overall		10-15	-15	25-30	25-30	30-40	10-15

n.a. = not available

Notes: Incentives are calculated for the first 10 years of operation. All economies are assumed to offer a 100 percent tax deduction for equipment import costs and a 5 percent research and development tax write-off. The effective tax rate is considered separately from generally available incentives and is based on current statutes as of September 2020. US reduction is based on a best-case scenario with incentives and agreements as of September 2020.

Source: Boston Consulting Group and Semiconductor Industry Association report (<https://www.semiconductors.org/wp-content/uploads/2020/09/Government-Incentives-and-US-Competitiveness-in-Semiconductor-Manufacturing-Sep-2020.pdf>).

Over the period 2020-24, disbursed and enacted cash grants by donor jurisdictions (not including tax credits, concessional loans, and other incentives), exhibit a different pattern between countries than rankings based on the OECD report (2014-18). Between 2020 and 2024, the United States and China were equally generous, the European Union even more so, but Japan gave relatively little, and Korea and Taiwan, none. But leading Korean and Taiwanese chip firms got substantial cash subsidies from other countries.

BCG and SIA Report on Fab Costs

Government incentives are a strong reason for substantial Asian chip production. Exhibit 8 of the 2022 BCG and SIA report contains striking comparative data, reproduced in part as table 8. The comparison evaluates the TCO in different national locations. TCO is calculated as capex plus cash operational expenses over a 10-year period, minus government incentives. According to a BCG analyst, the TCO estimates in Exhibit 8 were derived from a combination of published reports and corporate interviews. Whereas US incentives (both federal and state) reduced the TCO by 10-15 percent (pre-CHIPS Act), the reduction of TCO through South Korean and Taiwanese subsidies was estimated at 25-30 percent, and Chinese subsidies cut the TCO by 30-40 percent. Subsidies reduce TCO in Japan and Germany by about the same amount as in the United States.

NBER Working Paper

Pinelopi Goldberg and four colleagues have authored [NBER Working Paper 32651](#), which uses a new methodology to estimate national subsidies to the semiconductor industry over the period 2010-22. The NBER authors start with

Table 9

NBER working paper calculation of semiconductor policies in the Big 6 jurisdictions, 2010–22

<i>a. Counts of all semiconductor policies</i>						
Jurisdiction	European Union	United States	Japan	China	South Korea	Taiwan
Policy count	17	11	8	7	5	n.a.
<i>b. Monetary values of identified policies (billions of current US dollars)</i>						
Jurisdiction	China	South Korea	United States	Japan	European Union	Taiwan
Expenditure	509	78	42	16	16	n.a.

n.a. = not available

Note: Numbers in both panels are eyeball estimates from figure 3 in the National Bureau of Economic Research (NBER) Working Paper 32651 (<http://www.nber.org/papers/w32651>).

reports of trade-restrictive measures since 2009 (the global financial crisis) gathered by the [Global Trade Alert](#) (GTA). First, they extracted from the large GTA database episodes involving semiconductors. Then they turned to published news and industry reports to match government spending to the identified measures. Two results from figure 3 in the NBER working paper contrast with the other datasets summarized in this report.

First is a count of all policy interventions by originating countries over the survey period, shown in this report's table 9, panel a. By policy count, the largest is Europe (the sum of the Czech Republic, France, Germany, Italy, Netherlands, Malta, and the United Kingdom), followed by the United States, Japan, China, and South Korea, in that order. Policy interventions are also identified for several other countries not shown in table 9 (Brazil, Canada, India, Russia, Saudi Arabia, and Thailand). More interesting is that the GTA database reported no interventions by Taiwan, an obvious omission even though Taiwan's subsidies are comparatively light.

Second is the monetary value of identified policy interventions during the survey period, also shown in this report's table 9, panel b. Topping the list is China, including the provinces, at \$509 billion, followed by South Korea (\$78 billion), the United States (\$42 billion), Japan (\$16 billion), and the European Union (\$16 billion). Again, no monetary figure is reported for Taiwan, but India (not shown in table 9) is reported at \$18 billion, ahead of Japan.

Evidently, the rank order of the number of policy interventions differs sharply from the rank order of monetary values. This report assigns greater importance to monetary values. During the period 2010–22 (before the CHIPS Act and knock-on acts in South Korea, Japan, the European Union, and Taiwan), China was by far the largest subsidizer. Because of assorted limitations (recorded by Goldberg et al. and mentioned earlier in this report), huge subsidies did not translate into Chinese semiconductor leadership.

COMPARATIVE TAX RATES

American industrial policy advocates might worry that other Big 6 jurisdictions offer more generous tax incentives than the United States. However, [data](#) compiled by Horst on the statutory tax rates and ETRs paid by US and foreign multinational companies in several industries, including semiconductors, indicate that the United States is more generous taxwise than most other Big 6 jurisdictions. The [Horst dataset](#) reports the following tax rates:

- **Statutory tax rate** is the income tax rate that a corporation applies in its ETR reconciliation tables included in notes to its annual financial statements.
- **GAAP ETR** is the most widely used method of calculating a corporation's ETR. It is calculated as the ratio of the total provision for income taxes to earnings before tax (EBT) from continuing operations as reported on consolidated statements of income.
- **Normalized GAAP ETR** differs from the GAAP ETR because both the GAAP income tax provision and the GAAP EBT are adjusted to eliminate nonrecurring items of income or expense identified by S&P Capital IQ (the financial-statement database used by Horst).
- **Cash flow ETR** differs from the two GAAP-based ETR methods in that both the income tax expense and the EBT values under the cash flow ETR method are based on a corporation's consolidated statement of cash flows and thus do not include any accrued income or expenses.

Table 10 lists the 12 US and 7 foreign chip companies covered in the Horst dataset.

The foreign chip firms represent Europe, Japan, South Korea, and Taiwan, but no Chinese firms are covered. Reported tax rates are averages for the years 2018–23.

Median tax rates for US multinationals are, under all tax rate definitions, lower than median tax rates for the covered foreign multinationals. The statutory tax rate difference is almost 7 percent, but the more important ETR differences are in the 3–4 percent range. Thus, it appears that US chip firms have been marginally advantaged with respect to corporate taxes by comparison with foreign competitors, even though US R&D tax credits are skimpy. However, as a standout case, Intel paid a much higher cash flow ETR than other US or foreign firms. Importantly, Chinese chip firms are not covered and possibly they are tax advantaged relative to US chip firms.

COMPARISON OF DATASETS

The four sets of subsidy data described above reveal the difficulty of ranking countries according to the magnitude of their industrial incentives. The disparity between rankings based on direct grants (2020–24) and rankings based on comprehensive OECD measures (2014–18) shows that cash subsidies give an incomplete picture of government incentives. However, based on the four subsidy datasets and country sketches provided above, it is fair to conclude that China has given the most subsidies. Yet trade statistics indicate that China is far from enjoying the strongest competitive advantage. Among the other Big

Table 10
Semiconductor company tax rates

Corporation	Country of headquarters	Market cap, February 28, 2024 (billions of US dollars)	Statutory tax rate (percent)	GAAP ETR (percent)	Normalized GAAP ETR (percent)	Cash flow ETR (percent)
Nvidia Corporation	United States	1,911.44	22.40	0.50	3.20	7.90
Broadcom Incorporated	United States	597.54	21.20	-16.40	1.20	6.40
Advanced Micro Devices, Incorporated	United States	285.25	21.00	-15.50	-14.30	12.90
Intel Corporation	United States	177.53	21.00	9.90	9.10	31.70
Qualcomm Incorporated	United States	174.06	21.00	26.60	14.90	16.50
Texas Instruments Incorporated	United States	148.25	21.00	12.50	12.50	16.30
Micron Technology, Incorporated	United States	99.03	22.90	7.50	4.70	16.70
Analog Devices, Incorporated	United States	93.11	21.60	7.60	9.30	15.30
Microchip Technology Incorporated	United States	44.41	22.30	13.20	5.70	7.30
Marvell Technology, Incorporated	United States	58.39	32.00	-86.30	-65.10	6.30
ON Semiconductor Corporation	United States	32.68	21.00	14.90	15.70	20.00
Monolithic Power Systems, Incorporated	United States	34.13	21.00	12.80	12.90	12.70
Taiwan Semiconductor Manufacturing Company Limited	Taiwan	571.34	20.30	11.50	11.50	20.00
SK Hynix Incorporated	South Korea	81.39	27.80	30.00	29.20	99.40
MediaTek Incorporated	Taiwan	56.02	30.30	12.20	11.50	9.90
Infineon Technologies AG	Germany	46.85	28.00	17.50	18.30	18.30
NXP Semiconductors N.V.	Netherlands	62.57	25.50	12.40	10.30	14.10
STMicroelectronics N.V.	Switzerland	40.72	25.50	11.40	11.80	17.20
Renesas Electronics Corporation	Japan	29.84	31.50	24.10	24.70	13.90
Median: US multinationals	12	123.64	21.10	8.70	7.40	14.10
Median: Foreign multinationals	7	56.02	27.80	12.40	11.80	17.20
Difference between foreign and US multinationals			6.70	3.70	4.40	3.10

GAAP = Generally Accepted Accounting Principles; ETR = effective tax rate

Source: Thomas Horst, A Comparison of Effective Tax Rates for U.S. vs. Foreign Multinational Corporations, Tax Notes International, May 20, 2024, p. 1219 (<https://www.taxnotes.com/tax-notes-international/corporate-taxation/comparison-effective-tax-rates-u.s.-vs-foreign-multinational-corporations/2024/05/20/7ing8>).

6 jurisdictions, no clear subsidy ranking order emerges. What is clear is that the revealed competitive advantage of South Korea and Taiwan cannot be attributed to outsize subsidies. Human talent and smart corporate decisions better explain their success. As for corporate taxes, US-headquartered firms enjoy a marginal advantage over several competitors based in market economies but may be disadvantaged relative to Chinese firms (especially SMIC).

POSSIBLE SUBSIDIES, 2024-32

As the country sketches show, all Big 6 jurisdictions offer generous semiconductor subsidies, with ambitious aspirations. By 2030, the United States seeks to produce 20 percent of global advanced chips, up from 0 percent in 2024.²⁴ The Made in China 2025 plan seeks 70 percent self-sufficiency by 2025, even though chip imports were two times chip exports in 2023. The European Union seeks to produce 20 percent of world chips in 2030, up from 10 percent in 2021. Japan has not announced a percentage of world production goal but rather seeks excellence in advanced logic and memory chips, 2 nm and under. Without an announced goal, Taiwan is seeking to maintain its position as the world's leading pure-play foundry. South Korea plans to double exports (chiefly memory chips) from \$100 billion in 2020 to \$200 billion in 2030.

Big 6 jurisdictions are more wedded to target declarations than capping their subsidy programs. Jurisdictions can shift the composition of programs between tax credits, cash grants, concessional loans, and other inducements. With those aspirations and flexibility in mind, it is possible, perhaps even likely, that the Big 6 jurisdictions will provide a range of subsidies equivalent to 25 percent of world wafer capex by 2032, both for foundries and for other components of the semiconductor supply chain (R&D, ATP). In 2024 world wafer capex should be about \$150 billion; based on past experience, this should double by 2032 to \$300 billion annually. Assuming an average annual capex of \$225 billion, the cumulative eight-year total of world wafer capex could reach \$1.8 trillion. Total subsidies at 25 percent of capex would amount to \$450 billion over eight years, some \$56 billion annually.

Annual semiconductor subsidies of \$56 billion represent a substantial fiscal commitment, even spread over six jurisdictions. But since the paramount goal of each jurisdiction is to locate more of the world's fabs within its domestic territory, generous subsidies seem almost inevitable. A secondary goal, given greater prominence in some countries, is to advance the technology of logic and memory chips. A third goal, critical for the United States, is to maintain a large technological lead over China. The combination of goals promises a bright future for public subsidies, if not for private taxpayers.

24 Startling, however, is that the United States only seeks to increase its share of all global chip production—mature as well as advanced—by just 2 percent based on BCG and SIA calculations.

III. Evaluation of the US CHIPS and Science Act

The influential BCG and SIA report—which, together with *Chip War*, inspired the CHIPS and Science Act—complained that US semiconductor “manufacturing capacity” fell from 37 percent of the world total in 1990 to 12 percent in 2020. When the BCG and SIA report was published, the United States was forecast to add just **6 percent** of the new global manufacturing capacity that would be created between 2020 and 2030. These numbers alarmed US policy leaders.

National manufacturing capacity is not a revenue metric. Rather, it reflects the quantity of chips that could be produced by foundries located within national borders, if operated at full capacity. As the [Hufbauer-Hogan Policy Brief](#) showed, and as this report confirms, on revenue metrics the US performs far better than on manufacturing capacity metrics, both because US semiconductor firms earn substantial revenue from designing advanced chips and because US chips command premium prices.

The BCG and SIA report predicted that a significant industrial policy initiative (costing \$50 billion) would increase the US share to 24 percent (up from 6 percent) of the new global manufacturing capacity added between 2020 and 2030. As a result, in 2030 some **14 percent** of world manufacturing capacity would be located within US borders, up from 12 percent in 2020.

Given the prominence of the BCG and SIA report, Congress almost certainly had such forecasts in mind when the CHIPS Act was passed. In August 2022, upon signing the CHIPS Act, President Biden issued a [White House Fact Sheet](#) that lamented the fall in US chip production (measured by volume, not revenue) to 10 percent of the global total but did not forecast what percentage would be achieved by 2030.

In 2024, in the context of [announcing CHIPS Act awards](#), Secretary of Commerce Gina Raimondo stated that the United States would aim to produce **20 percent** of global “leading- edge” or “most advanced logic chips” by 2030. Formulating the US goal in these terms did not contradict previous White House statements but did represent a retreat from the BCG and SIA forecast of 14 percent of *all* chip manufacturing capacity by 2030. The reason for the discrepancy is that mature or legacy chips account for the dominant share of manufacturing capacity when measured in volume terms.

In announcing the Notice of Funding Opportunity (NOFO) for CHIPS Act awards in February 2023, the Department of Commerce offered [these definitions](#) of “leading-edge” or “most advanced” chips produced by “leading-edge facilities”:

- Advanced logic chips (described as below 5 nm or logic fabs using extreme ultraviolet patterning equipment).
- Advanced memory chips (3D Not-And [NAND] chips [they store memory without power] with 200 layers or more and DRAM chips at half pitch of 13 nm and below).

President Biden and congressional supporters of the CHIPS Act clearly intended that the technology, plus the physical and human capital required to produce advanced chips, should be located on American soil, whatever the cost. Because of acute chip shortages during the COVID pandemic (2020–22), coupled with apprehension over earthquakes and geopolitical hostilities, they were alarmed by US dependence on supply chains originating in Asia. However, CHIPS Act sponsors did not seriously consider alternative means of ensuring adequate supplies. Their laser focus was on constructing new fabs at home. One alternative, used for other critical materials, would have been the creation of revolving stockpiles managed by the Federal Emergency Management Agency (FEMA). Another alternative would have been financial incentives for US-based chip users to hold inventories much larger than customary. And a third alternative would have been financial incentives for foreign chip producers to maintain inventories within the United States. None of these alternatives entered the public debate.

In April 2024 Miller, author of *Chip War*, posted [an op-ed](#) in the *Financial Times* pronouncing the CHIPS Act a total success at a time when half of the \$39 billion grant money had been allocated to seven firms. Miller claimed that the subsidized projects would help insulate the United States from future chip shortages. He attributed all the planned capital outlays of the seven award-winning firms, then totaling some \$327 billion, to the CHIPS Act. In Miller's telling, the outlays would not have been made on US soil in the absence of federal subsidies.

While congressional and business supporters of the CHIPS Act likely subscribe to Miller's evaluation, this report takes a more critical "show me" approach. It asks two sets of questions. The first set is targeted at the explicit goals of the CHIPS Act and the stated aspirations of the Biden administration. The second set raises broader queries about US industrial policy for semiconductors.

CHIPS ACT GOALS AND ASPIRATIONS

The foremost goal of the CHIPS Act is to enhance economic and national security. This is to be achieved by manufacturing more chips in US territory, especially advanced logic and memory chips, whether by US firms or by firms based in allied countries. Cost is not the foremost consideration, although Secretary Raimondo [claimed](#) that US fabs will "produce advanced memory chips on economically competitive terms." For advanced memory chips, this was a reasonable forecast since Micron, based in Boise, Idaho, had already established itself as a low-cost producer well before the CHIPS Act. For logic and other advanced chips, the claim that US fabs will compete in price and performance with semiconductors made in Japan, Korea, or Taiwan remains to be demonstrated; fabs based in East Asia have long been leaders.

In its NOFO, the National Institute of Standards and Technology (NIST) stated that cash subsidies should normally fall in the range of [5-15 percent](#) of projected capital outlays. All the companies awarded cash subsidies (the so-called award firms) are expected to claim the 25 percent federal investment tax credit on eligible capital outlays and, if needed, can seek concessional loans under the CHIPS Act. In [an address to CSIS](#), Secretary Raimondo emphasized that CHIPS Act firms should be in production by 2030. She stressed advanced technology, saying that \$28 billion of the \$39 billion grant fund would be directed to “leading-edge” production, and that the United States would produce 20 percent of global leading-edge chips by 2030, up from 0 percent in 2024.

With that background in mind, five questions are explored in the following sections to probe goals and aspirations. Economic efficiency is set aside, both because the overriding objective is manufacture on US territory and because it is too early to assess how well newly constructed US fabs and ATPs will compete with East Asian facilities.

Question 1: Would CHIPS Act firms, or their domestic competitors, have invested to the same extent in US fabs without federal subsidies?

Answer: No.

In February 2023 the US Department of Commerce issued a [76-page document](#) summarizing application procedures for CHIPS Act grants and loans. Among numerous requirements, applicants should secure companion support from state or local sources (but no minimum is specified), they are expected to claim the 25 percent federal tax credit, and, importantly, the grant or loan must “incentivize” the chip project. It is worth mentioning that the CHIPS Act allows the government to [recapture](#) a portion of “windfall profits” earned by award firms.²⁵ The Department of Commerce’s CPO recruited some 150 experts to evaluate applications, some from Wall Street.

CPO personnel should be proficient at determining whether CHIPS Act support is decisive in enabling the applicant to carry out the project. That determination should hinge on whether the grant, coupled with the 25 percent investment tax credit and possible concessional loans, raises the expected return to meet or exceed the firm’s hurdle rate—namely, the minimum prospective return to justify a major capital outlay. As of August 2023 some [460 firms](#) had submitted “statements of interest” in a CHIPS Act award. As of October 2023 the number was over [500 firms](#). Corporate applications and CPO determinations are confidential. Hence, it is not possible for external reviewers, such as the authors of this report, to make a rigorous evaluation as to whether CHIPS Act grants, loans, and 25 percent investment tax credits were essential for each individual winning project.

Yet a broad assessment can be made of the chips manufacturing portfolio. The post-2019 burst in capital spending on US territory, documented in table 3, almost proves that the anticipation and realization of CHIPS Act subsidies (importantly including the investment tax credit) were essential for massively

²⁵ Windfall profits are defined by reference to the confidential financial projections submitted to the DOC by applicant firms. Presumably, the recapture provision will discourage firms from submitting overly gloomy projections.

stimulating investment. Chip manufacturing capex soared from well under \$10 billion annually prior to 2020 to \$80 billion in 2022, [with more ahead](#). We say “almost” because a strict policy of high tariffs on chip imports might have equally stimulated investment, but that option was never publicly considered by the Biden administration. During his 2024 campaign, however, president-elect Trump [said that tariffs](#) would have been superior to subsidies as a way to induce chip makers to build fabs in the United States. At this writing, it is unclear whether Trump will seek changes to or repeal of the CHIPS Act after he takes office in 2025. The subsidy package was an essential ingredient for large-scale construction of manufacturing plants on US soil without resorting to high tariffs.

The subsidy package has two distinct components: First, the Department of Commerce awards grants and loans after scrutiny of the applicant project’s merits, with an emphasis on its contribution to national security; and second, the applicant seeks the 25 percent investment tax credit for qualifying semiconductor construction, with no vetting by a government bureaucracy and no security condition. The investment tax credit is not refundable, but tax planning should enable most semiconductor firms to take full advantage of the credit.

Given this bifurcation of the subsidy package, the critical question is whether CHIPS Act grants and loans were needed for the winning projects, in addition to the automatic investment tax credit (in most cases, a larger subsidy than grants and loans combined). Based on the capex record, this report concludes that the investment tax credit was a necessary but not sufficient condition for the projects selected by the CPO to go forward. CPO experts make the determination that a grant, and possibly a loan, is essential to launch each winning project. That is the plain meaning of the Department of Commerce [commitment](#) to “incentivize” construction.²⁶ External evaluators, without access to detailed CPO spreadsheets, might conclude that CPO experts know their business, and that a grant (possibly supplemented by a concessional loan) was essential for each project granted an award.

This report is marginally skeptical, for two reasons. First, projects to produce mature or legacy chips will, almost by definition, produce chips for which more than one domestic firm possess the requisite technology. Hence, it is entirely possible that another domestic firm, not awarded a grant or concessional loan, could have produced the same mature chips incentivized solely by the 25 percent investment tax credit (and any state or local grants). Additionally, if the award firm has strong finances, it might have produced the chips solely on the basis of those incentives, without a CHIPS Act grant or concessional loan.

Second, projects to produce advanced or leading-edge chips, or advanced ATP services, almost by definition deploy unique technology. Accordingly, if the award firm has strong finances, it might have produced the chips, or supplied the ATP services, without a grant or concessional loan, but with the investment

26 A Department of Commerce [NOFO](#) contains this statement: “Second, funding is available to covered entities ‘to incentivize investment in facilities and equipment in the United States’ for the production of materials used to manufacture semiconductors or semiconductor manufacturing equipment. An applicant must demonstrate how the CHIPS Incentives requested will incentivize the applicant to make investments in facilities and equipment in the United States that would not occur in the absence of the CHIPS Incentives.”

Other [Notices of Funding Opportunity](#) contain the same statement.

tax credit, in the absence of compelling circumstances special to the case. If the award firm does not have strong finances, the grant or concessional loan might have been essential, along with the investment tax credit.

The summaries that follow detail the CHIPS Act awards in chronological order. (As a matter of information, the SIA has also published a [summary of awards](#).) Based on the foregoing points, in each case this report offers an evaluation as to whether the named firm, or a domestic competitor, might have carried out the project without a CHIPS Act grant (possibly supplemented by a concessional loan). The 25 percent investment tax credit (often supplemented by state and local grants) is assumed for each award-winning and alternative project. Therefore, some smaller projects might have been undertaken without a CHIPS Act grant or loan, though they would have an investment tax credit (possibly supplemented by state and local grants). However, for the larger projects, CHIPS Act grants might have been essential.

As of October 17, 2024, the Department of Commerce had signed preliminary memoranda of terms for 20 projects, with total contemplated grants of \$33 billion plus concessional loans. That leaves a few billion more to be awarded. To conclude this report in a timely manner, no projects after the first 20 are evaluated.

Project 1. BAE Systems Electronic Systems

On December 11, 2023, the Department of Commerce and BAE Systems Electronic Systems [signed a preliminary memorandum of terms](#) (PMT) to provide the company with approximately \$35 million in grants under the CHIPS Act to support modernization of the company's Microelectronics Center (MEC) in Nashua, New Hampshire, characterized by the Department of Commerce as a mature-node production facility. The project will replace aging tools and quadruple the production of chips [for military purposes](#), including F-15 and F-35 fighter jets. The Department of Commerce press release did not mention concessional loans or incentivized capital outlays. A [news story reported](#) that 30 additional jobs would be added to the 200-person workforce over the next five years.

[According to BAE](#), the MEC is a Department of Defense-accredited semiconductor chip fab that produces advanced semiconductors to meet military specifications beyond chips available commercially. It is one of the few 6-inch wafer foundries that make gallium arsenide and gallium nitride high-electron-mobility transistors.

BAE Systems Electronic Systems is a subsidiary of the British firm BAE Systems, which specializes in defense contracts and has multiple US locations. The subsidiary reports [31,600 employees](#) in all US locations, with [6,000](#) in various New Hampshire facilities and [200](#) at the MEC plant.

In 2023 consolidated revenue of the parent firm and its multiple subsidiaries was \$28.7 billion, with operating income before depreciation of \$3.9 billion. Market capitalization in June 2024 was \$52 billion, and BAE shares [traded at 22 times](#) trailing earnings.

Financial details for BAE Systems Electronic Systems are not publicly available, but the foregoing information indicates that the corporate group

appears financially strong. An award of \$35 million is very small compared with group revenue or operating income.

The semiconductors in question are largely destined for the military. The Pentagon has historically been a generous purchaser of specialized semiconductors, and it seems likely that prices could be substantially raised if shortages threatened to delay F-35 fighter jets or other defense projects. Even a price increase of 200 percent would be a very small item in the multibillion budget for defense hardware.

The Department of Commerce announcement characterizes the chips as mature, and the BAE announcement emphasizes their special characteristics. That phrasing suggests another US firm might step in as a supplier if BAE Systems Electronic Systems did not modernize and enlarge its capacity. It seems likely that among other US chip firms, at least one or two might have produced the same 6-inch wafer at premium prices for military use.

In this report's view, given the apparent strength of BAE finances, the mature character of the chips, and the deep pockets of the Pentagon, the CHIPS Act grant probably was not essential to secure reliable domestic supplies.

Project 2. Microchip Technology

On January 4, 2024, the Department of Commerce and Microchip Technology signed a [PMT](#) to provide the company with approximately \$162 million in grants for Microchip to increase US production of "mature-node" semiconductors for automotive, commercial, industrial, defense, and aerospace industries. The proposed CHIPS funding will be split across two projects: approximately \$90 million to expand a fabrication facility in Colorado Springs, Colorado, and approximately \$72 million to expand a fabrication facility in Gresham, Oregon. The Department of Commerce announcement did not mention concessional loans. The projects should nearly triple the output of semiconductors at these sites and create approximately 700 construction and manufacturing jobs.

In February 2024 Microchip announced [plans to invest \\$880 million](#) to expand its silicon carbide and silicon production capacity at its Colorado Springs facility, installing technology to run on 8-inch wafers instead of 6-inch wafers. In March 2024 the firm announced [it was halfway](#) on its \$800 million project to [triple production capacity](#) at the Gresham facility. The two projects contemplate capital outlays of \$1.68 billion. Assuming all outlays are eligible for the 25 percent investment tax credit, the additional subsidy will be \$420 million, substantially more than the cash grants.

Influential congressman Earl Blumenauer (D-OR) characterized semiconductors produced at the Gresham facility [as legacy chips](#). These were in short supply [during the pandemic](#), an experience that helped inspire the CHIPS Act.

Microchip Technology revenue for fiscal 2023 (June 2023–March 2024) was \$8.4 billion, with operating income before depreciation of \$4.1 billion. Market capitalization in June 2024 was \$50 billion, and shares [traded at 27 times](#) trailing earnings.

The characterization in the Department of Commerce and Blumenauer announcements that Microchip Technology specializes in mature-node and legacy chips indicates that another domestic firm could have increased its

production solely on the basis of the investment tax credit. Microchip's own announcement stated that major expansion programs both for Colorado Springs and Gresham were under way with corporate funding when the CHIPS Act award was announced, indicating the firm's financial strength.

In this report's view, the CHIPS Act grant of \$162 million might not have been essential to ensure domestic production of the mature chips produced in Colorado and Oregon.

Project 3. GlobalFoundries

On February 19, 2024, the Department of Commerce and GlobalFoundries signed a [PMT](#) to provide approximately \$1.5 billion in grants under the CHIPS Act to produce current-generation and mature semiconductors. In addition to grants, the Department of Commerce will extend [\\$1.6 billion](#) of concessional loans to GlobalFoundries. Based on Congressional Budget Office estimates, the expected loss factor for CHIPS Act loans is 8 percent. Taking this figure as a conservative estimate of the concessional subsidy, the additional benefit to GlobalFoundries is about \$130 million. Grants and loans will support a new state-of-the-art facility, expand existing capacity, and modernize GlobalFoundries fabs in New York and Vermont that produce chips for automotive, communications, and defense industries. Collectively, the new facilities are projected to cost \$12.5 billion, creating [9,000 construction jobs and 1,500 manufacturing jobs](#). The 25 percent investment tax credit on \$12.5 billion capital outlays (assuming all outlays are eligible) adds \$3.1 billion to the subsidy figure.

Capacity expansion and a new facility will be located in [Malta, New York](#), tripling the firm's manufacturing capacity in New York over a decade. The expansion will primarily produce chips for the [auto industry](#). The new facility will produce [300 mm \(12-inch\) "high value" wafers](#) not currently made in the United States. A fab in Burlington, Vermont, will be [updated to manufacture 200 mm \(8-inch\) gallium nitride wafers](#) not currently made in the United States [but used for](#) electric vehicles, the power grid, and smartphones.

GlobalFoundries revenue for 2023 was reported as \$7.4 billion, with operating income before depreciation of \$2.6 billion. Market capitalization in June 2024 was \$28 billion, and shares [traded at 31 times](#) trailing earnings.

GlobalFoundries enjoys a strong financial position. The combined subsidy represented by CHIPS Act grants and concessional loans, some \$1.7 billion, amounts to about 6 percent of its market cap and about 65 percent of 2023 operating earnings. The 25 percent investment tax credit prospectively adds another \$3.1 billion subsidies, enough to bring the total subsidy package to \$4.8 billion, some 17 percent of market cap and almost two years' worth of operating earnings. Without the investment tax credit, the two projects appear to be an oversized risk for GlobalFoundries. However, the added subsidy from grants and concessional loans might not have been needed.

In this report's view, while it is a close call, the CHIPS Act grants and loans probably were not essential for the two GlobalFoundries plants.

Project 4. Intel

On March 20, 2024, the Department of Commerce and Intel signed a [PMT](#) to provide the company with up to \$8.5 billion in CHIPS Act grants to produce leading-edge logic chips for purposes such as AI and to create an advanced packaging facility. In November 2024, the Department of Commerce [reduced](#) the grant to \$7.9 billion. In addition, the CHIPS program will provide up to \$11 billion in concessional loans to Intel, implying a subsidy of about \$0.9 billion (8 percent of loan amount).

Over the next five years, Intel expects its US chip investments to surpass \$100 billion as it expands in Arizona, New Mexico, Ohio, and Oregon. New manufacturing jobs are estimated at over 10,000 and construction jobs at 20,000. If the 25 percent investment tax credit can be claimed for all capital outlays, the additional subsidy will be \$25 billion. All told, CHIPS Act grants and the concessional element of loans, together with investment tax credits, bring the subsidy package to \$34.4 billion, almost 35 percent of planned capital outlays. [Available data](#) on plant location and purposes are summarized as follows:

- **Chandler, Arizona:** Construction of two new leading-edge logic fabs and modernization of an existing fab, to produce the company's most advanced chip design, the Intel 18A chip. In 2022 Intel and Maricopa Community Colleges launched a first-of-its-kind program with Intel instructors to train students as semiconductor technicians. The Chandler investment will support 3,000 manufacturing jobs and 6,000 construction jobs.
- **Rio Rancho, New Mexico:** Two fabs will be modernized as advanced packaging facilities, creating the largest advanced packaging facility in the United States. The Rio Rancho investment will support [700 manufacturing jobs and 3,000 construction jobs](#).
- **New Albany, Ohio:** Two leading-edge logic fabs will be created. To help ensure a skilled workforce, Intel has funded over 80 institutions of higher education across the state. In 2022 Intel said that its initial investment in Ohio was \$20 billion, but the firm could eventually spend as much as \$100 billion on the site. The New Albany investment planned with CHIPS Act money will support 3,000 manufacturing jobs and 7,000 construction jobs.
- **Hillsboro, Oregon:** Investment in frontier technology development facilities that will utilize the world's first high numerical aperture (NA) extreme ultraviolet (EUV) lithography equipment. Additionally, the Gordon Moore Park campus in Hillsboro will undertake frontier semiconductor R&D. The Hillsboro investment will support several thousand manufacturing and construction jobs.

At the announcement, Secretary Raimondo said Intel investments will put the United States "[on track](#)" to produce 20 percent of the world's "leading-edge" chips by 2030, up from 12 percent in 2024. But Intel CEO Gelsinger said that Congress would need to pass additional funds to continue bolstering the industry, without specifying a dollar amount. "It took us [three plus decades](#) to lose this industry. It's not going to come back in three to five years," Gelsinger said.

Intel revenue in 2023 was reported as \$54 billion, with operating income before depreciation of about \$10 billion. Market capitalization in June 2024 was \$130 billion, and shares [traded at 32 times](#) trailing earnings. Taking depreciation into account, Intel has [reported losses](#) in recent years. In August 2024, Intel announced [layoffs](#) of 15,000 workers, about 15 percent of global payroll.

Intel is a pioneer semiconductor producer and a megacap firm. Nevertheless, Intel's operating income as a percentage of revenue is modest for a chip company, and recent layoffs indicate the firm faces financial stress. Moreover, unlike most other large US chip firms, Intel's share price lost half its value between December 2023 and December 2024, when CEO Pat Gelsinger [was fired](#). It seems highly unlikely that Intel would invest heavily in US fabs for advanced logic chips and frontier high NA EUV technology facilities without the CHIPS Act grant and concessional loan, on top of the 25 percent investment tax credit. For advanced logic chips, the two major alternatives to Intel are TSMC and Samsung. It seems doubtful that those two firms would further enlarge their already ambitious plans for US chip production if Intel cut back on its CHIPS Act expansion. Both TSMC and Samsung already face the prospect of substantially higher manufacturing costs for their US fabs than fabs in Taiwan and South Korea.

In this report's view, the CHIPS Act grant and loan might have been essential for the Intel projects.

Project 5. TSMC

On April 8, 2024, the Department of Commerce and TSMC Arizona (a subsidiary of TSMC), signed a PMT to provide [up to \\$6.6 billion](#) in grants and up to \$5 billion in concessional loans (implying a further subsidy of \$0.4 billion) to support TSMC's three greenfield fabs to produce advanced logic chips in Phoenix, Arizona, entailing total investment of more than \$65 billion by 2030. In November 2024, DOC [confirmed](#) the grant and loan. At 25 percent, the investment tax credit subsidy could amount to \$16.3 billion, bringing the total subsidy package to \$23.3 billion. TSMC's projections of Arizona investment outlays have been progressively increased from \$12 billion in 2020 to \$40 billion in 2023 to \$65 billion in 2024. The subsidy package [amounts to 36 percent](#) of planned capital outlays. As mentioned, in February 2024 Secretary Raimondo forecast that the United States would produce [20 percent](#) of the world's most advanced logic chips by 2030.

TSMC already manufactures some 90 percent of the world's advanced logic chips. The first Arizona fab will produce [4 nm fin field-effect transistors \(FinFET\)](#) chips with multiple gates. That fab was announced during the Trump administration in May 2020, but at the time TSMC said [subsidies would be needed](#) to complete the fab. The second fab will produce 2 nm and 3 nm chips, and the third fab will tentatively produce [2 nm or more advanced chips](#), depending on demand. Currently, 3 nm chips are popular for AI, but Nvidia and other users [are migrating toward](#) 2 nm chips.

TSMC Arizona will create approximately 6,000 direct manufacturing jobs and more than 20,000 construction jobs. However, TSMC's production plans have been delayed by a shortage of qualified workers. Completion of the first fab [was](#)

delayed from 2024 to 2025, and startup for the second fab will be delayed from 2026 to 2028. Meanwhile, TSMC will likely complete [three 2 nm fabs](#) in Taiwan and export the chips to the United States.

TSMC revenue in 2023 was reported as \$71 billion, with operating income before depreciation of \$47 billion. Market capitalization in April 2024 was \$741 billion, and shares traded at 27 times trailing earnings.

TSMC was a pioneer of the pure-play foundry in 1987 and has become the dominant global producer of advanced 3 nm and 2 nm chips. TSMC manufacturing technology is superior to almost all rivals. By market capitalization, TSMC is today surpassed only by Nvidia, but it is closely followed by Broadcom. If so inclined, TSMC could easily construct the three Arizona fabs without CHIPS Act subsidies and investment tax credits. However, TSMC executives have clearly stated that US construction costs are substantially higher than in Taiwan, and US wage rates clearly exceed Asian levels. Without subsidies, TSMC would not have committed to three Arizona fabs and investment outlays of \$65 billion. The same logic would equally deter the next most likely producer of advanced chips, Samsung.

To be sure, Taiwan and TSMC are acutely aware of their security dependence on the United States, and they understand the US determination to construct advanced logic chips on US territory. In the absence of CHIPS Act subsidies, the threat of harsh US tariffs—strongly opposed by industry producers and consumers alike—might have forced TSMC to invest in US plants.

In this report's view, the CHIPS Act grant and loan probably were essential to lure TSMC to produce in America without the threat of hostile measures.

Project 6. Samsung

On April 15, 2024, the Department of Commerce and Samsung Electronics (Samsung) signed a [PMT](#) to provide up to \$6.4 billion in grants to support the production of advanced logic chips, fully depleted silicon-on-insulator (FD-SOI) process technologies, and R&D facilities. No concessional loans were mentioned. Samsung's capex for the projects are projected at [\\$45 billion](#), roughly double the outlays announced by Samsung in 2021. At 25 percent, the investment tax credit could add \$11.3 billion to the subsidy package, making a subsidy total of \$18 billion, some [40 percent](#) of projected capital outlays. At the announcement, Secretary Raimondo repeated the US goal to produce 20 percent of world advanced logic chips by 2030. Over the next five years, Samsung projects will create 17,000 short-term construction jobs and 4,500 permanent manufacturing jobs:

- **Taylor, Texas:** Construct two advanced logic foundry fabs to manufacture 4 nm and 2 nm chips, plus an R&D facility for next-generation technology and an advanced packaging facility for 3D high-bandwidth memory (HBM) and 2.5D packaging. These projects will serve AI and the communications, automotive, and defense industries.
- **Austin, Texas:** Expand an existing facility to produce FD-SOI technologies for the aerospace, defense, and automotive industries. This facility will collaborate with the Department of Defense. FD-SOI technology is particularly good for [radio applications](#).

After TSMC, Samsung is the leading producer of advanced logic chips (4 nm, 3 nm, and 2 nm). Unlike pure-play TSMC, Samsung is an integrated device manufacturer, meaning it both designs and manufactures chips. Like TSMC, Samsung operates fabs worldwide, including in China. In 2023, Samsung's global revenue was **\$194 billion** and its operating profit was **\$5 billion**, a poor result. In June 2024, Samsung's market capitalization was **\$386 billion**, and the trailing price/earnings ratio for shares was **14.6**.

Samsung enjoys a strong financial position. But while its revenues were more than twice the level of TSMC, Samsung is not as strong financially as TSMC, and its market capitalization is about half the size of TSMC. Even so, Samsung could build the Texas plants without a CHIPS Act grant. Samsung is well aware of the US military alliance with Korea and US security concerns. But capital outlays for a fab and annual production costs are much higher in Texas than in Korea. Given those facts, and the absence of hostile US tariff threats, Samsung would not have committed to two new fabs in Texas without the CHIPS Act grant. The alternative producer is TSMC, but for the same reasons, TSMC would not double down on its US commitment if Samsung canceled its investment in Texas.

In this report's view, the CHIPS Act grant might have been essential to lure Samsung to produce in America.

Project 7. Micron

On April 25, 2024, the Department of Commerce and Micron Technology signed a PMT to provide up to \$6.1 billion in grants and \$7.5 billion of concessional loans (implied subsidy of \$0.6 billion) to produce advanced memory semiconductors. The Department of Commerce **confirmed** the grant in December 2024. The CHIPS Act subsidies will support two DRAM fabs in New York over the next two decades, costing approximately \$100 billion, and one DRAM fab in Idaho, costing about \$25 billion. About \$50 billion of total capital outlays will be spent over the next six years. Assuming Micron is only able to claim the 25 percent investment tax credit for capex over the next six years, the additional subsidy is \$12.5 billion, making a total subsidy package of \$20.6 billion, about 42 percent of planned capital outlays over the next six years. The new fabs will further Micron's plan to onshore approximately 40 percent of its DRAM chip production over the next two decades. Together, the three fabs are projected to create **9,000 short-term construction jobs and 11,000 permanent manufacturing jobs**:

- **Clay, New York:** Construct the first two fabs of a planned four fab "megafab." The megafab was **announced earlier** in 2022. Each fab will have 600,000 square feet of clean rooms, totaling 2.4 million square feet across all four facilities, a record for the United States. The project will create **4,500 short-term construction jobs and 9,000 permanent manufacturing jobs**.
- **Boise, Idaho:** Construct a high-volume manufacturing fab, with approximately 600,000 square feet of clean room space to produce advanced DRAM chips. The fab would be located near Micron's R&D facility to improve efficiency. The project will create 4,500 short-term construction jobs and 2,000 manufacturing jobs.

Micron is the only US-based manufacturer of memory chips, competing in world markets with TSMC, Samsung, SK Hynix, and Chinese firms. Micron's latest HBM chips (HBM3E) are integrated with Nvidia's H200 GPUs, which power AI data centers and are a leading contributor to Micron's current profitability.

Micron revenue for the 12 months ending in fiscal 2023 was \$15.5 billion (a sharp drop from \$30.8 billion in fiscal 2022), and operating income before depreciation was \$3.3 billion, about 21 percent of revenue. Market capitalization in June 2024 was \$170 billion, and trailing earnings were negative.

Given its modest ratio of operating income to revenue and its negative earnings, it seems unlikely that Micron would have committed to \$50 billion of capex over the next six years without the CHIPS Act grant and loan. No other US-based firm makes advanced memory chips. The alternative to Micron would be continued memory chip imports from East Asia or production in the United States by TSMC, Samsung, or SK Hynix.

In this report's view, the CHIPS Act grant and loan might have been essential to enlarge Micron's production of memory chips. An equivalent subsidy package might have been required to attract TSMC, Samsung, or SK Hynix to produce the same memory chips in America.

Project 8. Polar Semiconductor

On May 13, 2024, the Department of Commerce and Polar Semiconductor signed a PMT to provide grants up to \$120 million to double the firm's production of sensor and power chips within two years. These are legacy chips. The foundry is located in Bloomington, Minnesota, and the state will provide an additional \$75 million for capital outlays projected to total \$525 million. The firm will claim the 25 percent investment tax credit for eligible outlays, making an additional subsidy of \$131 million. The total subsidy package, federal and state, amounts to \$326 million, some 62 percent of planned capital outlays. The project will create 160 construction and manufacturing jobs.

Polar equity is currently 70 percent owned by Japanese firm Sanken Electric and 30 percent by Sanken's US subsidiary, Allegro MicroSystems, but will become US controlled through new equity investments of \$175 million, amounting to 59 percent of equity, by Niobrara Capital and Prysm Capital.

Polar is a small company but not publicly traded. Information is not available on its revenue or operating income. Based on the new equity investment, the firm's market cap is about \$300 million. Surya Iyer, CEO of Polar, stated that public support was essential for the firm to double production in two years. Given Polar's small market cap, that seems accurate.

While the CHIPS Act grant might have been essential for Polar to expand, similar chips could be produced by other firms on US territory without the CHIPS Act grant.

In this report's view, the CHIPS Act grant to Polar might not have been essential for the sensor and power chips to be produced in the United States.

Project 9. Absolics

On May 13, 2024, the Department of Commerce and Absolics, an affiliate of the Korean firm SKC with investment by Applied Materials, signed a PMT to provide grants up to \$75 million for an ATP plant to be built in Covington,

Georgia. Though no figure was cited for the total ATP investment, Department of Commerce guidelines call for cash grants to not exceed 15 percent of plant outlays, suggesting outlays of at least \$500 million, indicating a subsidy of \$125 million from the 25 percent investment tax credit. In November 2022, Absolics announced planned investment of **\$600 million** in Covington to produce a novel glass substrate for semiconductors. This planned outlay, coupled with the addition of an ATP plant, may have justified the CHIPS Act award. The new ATP plant is expected to provide jobs for 1,000 construction workers and 200 permanent employees. The firm will draw on Korean technology for advanced ATP techniques to manufacture 3D packages.

In December 2023 SKC had a **\$4 billion** market cap and no earnings. Given the parent firm's small size and poor earnings record, the cash grant is probably essential for Absolics to build an ATP plant. However, SK Hynix **announced in April 2024** that it would build its own \$3.87 billion ATP plant in Indiana without a CHIPS Act grant. Subsequently, SK Hynix was awarded a grant.

While the ATP industry is concentrated in Asia, SK Hynix would supply domestic ATP services in the absence of the grant to Absolics.

In this report's view, the CHIPS Act grant to Absolics might not have been essential for advanced ATP services on US territory.

Project 10. Rocket Lab

On June 11, 2024, the Department of Commerce and Rocket Lab signed a nonbinding PMT to provide up to **\$23.9 million** in grants to modernize and enlarge facilities for space-grade solar cells that power spacecraft and satellites. The project would increase Rocket Lab's production by 50 percent within three years and add 100 new manufacturing jobs. Based in Albuquerque, New Mexico, Rocket Lab is one of two US companies that specialize in making radiation-resistant compound semiconductors (space-grade solar cells) used in the James Webb Space Telescope and NASA's Artemis lunar explorations. Concessional loans were not announced, but Rocket Lab will apply for the federal 25 percent investment tax credit. The state of New Mexico will provide additional incentives worth **\$25.5 million**. While projected total capital outlays were not announced, the size of the CHIPS Act, grant coupled with Department of Commerce guidelines, suggests a figure of about \$150 million, indicating investment tax credits of about \$37 million.

Rocket Lab is a small company with 400 total employees, 2023 revenue of \$245 million, negative operating income (\$179 million loss), and negative earnings per share. Market capitalization in July 2024 was about **\$2.5 billion**. In light of Rocket Lab's small size and negative operating income, it seems unlikely that the firm would have embarked on the modernization and expansion project without the CHIPS Act grant and New Mexico's support.

The existence of another US company making space-grade solar cells, and the very large federal budget for space activity, indicate that supplies might have been found (perhaps at high prices) in the absence of Rocket Lab production.

In this report's view, the CHIPS Act grant probably was not essential for the production of space-grade solar cells on US territory.

Project 11. Entegris

On June 26, 2023, the Department of Commerce and Entegris signed a nonbinding PMT to provide up to **\$75 million** in grants to onshore semiconductor supply chains for advanced membranes, chemical filters, chemical storage drums, and specialized containers for silicon wafers. Entegris plans capital outlays of \$600 million for the manufacturing center located in Colorado Springs. It will employ 600 direct manufacturing workers and 500 construction workers. Concessional loans were not announced, but Entegris will seek the 25 percent investment tax credit, indicating an additional subsidy of \$150 million.

Entegris has **operations** in Europe and the Asia-Pacific region as well as the United States. It reported revenue of **\$3.5 billion** in 2023 and operating earnings of \$942 million. Market capitalization in July 2024 was \$19.8 billion, and shares traded at 63 times earnings. In light of the firm's size and profitability, Entegris could have financed the new manufacturing plant without the CHIPS Act grant. However, Entegris operations abroad, especially in the Asia-Pacific region, likely supply its suite of precursor semiconductor materials and equipment at a low cost.

In this report's view, the CHIPS Act grant might have been essential to persuade Entegris to build a new manufacturing center in the United States, thereby onshoring this supply chain. Alternative US suppliers are not mentioned in the Department of Commerce announcement.

Project 12. Rogue Valley Microdevices

On July 1, 2024, the Department of Commerce and Rogue Valley Microdevices (RVM) signed a nonbinding PMT to provide up to **\$6.7 million** in grants to expand a pure-play microelectromechanical systems and sensor foundry facility for 300 mm wafers in Palm Bay, Florida. No federal concessional loan was announced, but the Florida Department of Commerce will provide a \$5 million loan, and another \$3.2 million of subsidies will come from other state grants. RVM will seek the federal 25 percent investment tax credit, an additional subsidy of \$6.3 million. Capital outlays of \$25 million, supported by the various federal and state subsidies, are estimated to nearly triple RVM's manufacturing capacity and employ an additional 75 workers.

RVM is a small company, without publicly traded shares. Financial information is only available behind a paywall from sources like Dun & Bradstreet. Federal and state subsidies were probably essential for the firm to expand its pure-play foundry. However, the 300 mm mature-mode wafers produced by RVM will likely be available from GlobalWafers, the next CHIPS Act project.

In this report's view, the CHIPS Act grant might not have been essential for the production of 300 mm wafers by RVM on US territory, given the presence of GlobalWafers.

Project 13. GlobalWafers

On July 17, 2024, the Department of Commerce and GlobalWafers America signed a nonbinding PMT to provide up to **\$400 million** in grants to onshore production of 300 mm silicon wafers and SOI wafers. GlobalWafers, the parent company, is based in Taiwan. Current production of 300 mm wafers

is dominated by five firms, with 90 percent manufactured in Asia. US capital outlays of \$4 billion are anticipated, divided between production sites in Texas and Missouri. The two projects will create 1,700 construction jobs and 880 direct manufacturing jobs. Concessional loans were not announced. Presumably GlobalWafers America will seek the 25 percent investment tax credit, entailing an additional \$1 billion subsidy.

- **Sherman, Texas:** GlobalWafers will build the first 300 mm silicon wafer manufacturing facility for advanced chips in the United States. These wafers are key inputs for leading-edge, mature-node, and memory chips. The existing silicon epitaxy wafer facility in Sherman will be converted into silicon-on-carbide epitaxy wafers, used in high-voltage applications.
- **St. Peters, Missouri:** GlobalWafers will build a new plant for 300 mm SOI wafers. SOI wafers perform in harsh environments common in defense and aerospace end uses.

GlobalWafers reported **\$2.1 billion** revenue in 2023 and \$0.6 billion operating income. Market capitalization in July 2024 was **\$7.5 billion**, and shares traded at 12 times earnings. GlobalWafers may not have the financial resources to build the two US plants without the CHIPS Act grant. Current production costs are almost certainly lower in its Asian 300 mm factories than anticipated costs in the US factories. Extensive subsidies were probably essential to lure GlobalWafers to establish the new US foundries. The only alternative firms for new US foundries on this scale were other Asian semiconductor giants like TSMC and Samsung. They would also require extensive subsidies to expand their US facilities.

In this report's view, the CHIPS Act grant to GlobalWafers might have been essential to produce 300 mm silicon wafers on US territory.

Project 14. Amkor Technology

On July 26, 2024, the Department of Commerce and Amkor Technology signed a nonbinding PMT to provide up to **\$400 million** in grants and \$200 million in concessional loans (implying an additional subsidy of \$16 million) for a greenfield plant in Peoria, Arizona, to produce advanced packaging. Among **prospective users** are a nearby TSMC plant that will produce chips for Apple. The project is expected to require \$2 billion capex, to be **completed by 2027**, and Amkor will seek the 25 percent investment tax credit, another \$500 million subsidy. Total subsidies, including grants, loans, and tax credits are around \$900 million. The project will create 2,000 jobs, but the breakdown between construction and permanent jobs was not announced.

In 2023 Amkor had **revenues** of \$6.5 billion and operating income of \$470 million. In August 2024 Amkor's **market capitalization** was \$7.5 billion, and shares traded at 20 times earnings. Amkor **headquarters** are in Tempe, Arizona, but the firm has advanced packaging and testing operations worldwide, including Asia and Europe, and global employment is 28,700. Because ATP operations in Asia are cheaper than prospective US costs, the CHIPS Act grant and loan were probably essential for Amkor to launch the new plant in Peoria.

The most obvious alternative US source for ATP services is the prospective \$4 billion [SK Hynix plant](#) in Indiana, previewed in 2022 and awarded a CHIPS Act grant in August 2024.

In this report's view, because the SK Hynix plant is under way, the CHIPS Act grant and loan to Amkor might not have been essential to ensure advanced ATP facilities on US soil.

Project 15. SK Hynix

On August 6, 2024, the Department of Commerce and SK Hynix signed a nonbinding PMT to provide up to [\\$450 million](#) in grants to establish an HBM advanced packaging fabrication and R&D facility. The grant supports SK Hynix's investment of approximately \$3.87 billion in West Lafayette, Indiana, previewed in July 2022 but [definitively announced](#) in April 2024. The project will create approximately 1,000 jobs. The SK Hynix R&D facility will partner with Perdue University. SK Hynix will be eligible for up to \$500 million in concessional loans (a subsidy value of \$40 million). SK Hynix will be eligible for the investment tax credit on its total investment of \$3.87 billion, adding an additional subsidy of \$968 million.

SK Hynix reported revenue of [\\$21 billion](#) for 2023 (based on the year-end exchange rate of KRW 1295 = \$1). That was not a good year, and the firm experienced an operating loss of about \$4 billion. Although SK Hynix is a leader in advanced packaging, the field is competitive, and margins are typically low compared to design or fabrication. Market capitalization of common stock in December 2023 was about [\\$42 billion](#), about 14 percent less than at the end of 2022.

While SK Hynix has ample capital, recent poor operating results probably necessitated ample subsidies for the firm to commit almost \$4 billion to a new facility in Indiana. Additionally, prospective US operating costs for an advanced packaging plant are almost certainly higher than in Korea. The same obstacles probably confront alternative East Asian suppliers of advanced ATP services.

In this report's view, while it is a close call, the CHIPS Act grant and loan might have been essential.

Project 16. Texas Instruments

On August 16, 2024, the Department of Commerce and Texas Instruments signed a nonbinding PMT to provide a [\\$1.6 billion](#) grant and \$3 billion concessional loan (subsidy \$240 million) for the production of current-generation and mature-node chips (foundational chips) in two new fabs in Sherman, Texas, and one new fab in Lehi, Utah. Each of the three fabs will produce 300 mm wafers, making a significant addition to US domestic production of 300 mm wafers. Capital expenditures for the three fabs are projected to reach \$18 billion by 2030 (implying \$4.5 billion investment tax credits), creating 2,000 permanent jobs and a large number of construction jobs. Based on the relationship between capex and construction jobs in other large projects (such as GlobalFoundries, Intel, TSMC, Samsung, Micron, and Wolfspeed), the construction jobs for Texas Instruments' project are estimated to be around 9,500. The major justification for the CHIPS Act grant and concessional loan was shortages of foundational chips during the pandemic years.

Texas Instruments reported revenue of \$17.5 billion in 2023 and operating income of \$8.6 billion. Market capitalization was \$154 billion in December 2023, and shares traded over 30 times earnings. Subsidies through the CHIPS Act grant and concessional loan work out to about 10 percent of projected capital expenditures.

In this report's view, the 25 percent investment tax credit was probably critical for Texas Instruments to launch three new fabs. But, given the firm's robust financial strength, the grant and concessional loan might not have been essential.

Project 17. HP

On August 27, 2024, the Department of Commerce and HP signed a nonbinding PMT to provide a **\$50 million** grant to support, among other purposes, the manufacture of silicon devices for life sciences lab equipment used in drug discovery, single-cell research, and cell line development at the firm's facilities in Corvallis, Oregon. According to the accompanying [HP announcement](#), the grant will enable the firm to modernize and expand its microfluidics technology facility, which studies the control of fluid on a microscopic scale. No figures were reported for projected capex, but 150 construction jobs and 100 manufacturing jobs are expected. No concessional loan was reported.

In fiscal 2023 HP reported revenue of \$53.7 billion and operating income of \$5.1 billion. Market capitalization was \$30 billion in December 2023, and shares traded at about 11 times earnings. Obviously, the \$50 million grant is well within the firm's own financial capability. However, the project description has a strong R&D flavor. Semiconductor R&D is characterized by high risk and high reward (for the few successful ventures).

In this report's view, because of the R&D aspect of the project, the grant might be essential for HP to modernize and expand its facility. HP's unique microfluidics technology suggests that no other domestic firm could have undertaken a similar project.

Project 18. Edwards Vacuum

On October 10, 2024, the Department of Commerce and Edwards Vacuum signed a nonbinding PMT to provide an **\$18 million** grant to manufacture specialized dry vacuum (no oil) pumps in Genesee County, New York. Neither a concessional loan nor capex were announced, but the facility will create 600 permanent jobs. Dry vacuum pumps are a key component of semiconductor fabs. The Genesee County plant is the first manufacturing facility for these pumps on US territory. The facility was initially announced in 2022, well before the CHIPS Act grant.

Edwards Vacuum is a [British company](#), and, in turn, a subsidiary of the Swedish multinational firm Atlas Copco. Atlas Copco reported revenue of \$17.2 billion in 2023 and operating income of \$4.6 billion. Market capitalization was \$80.1 billion in December 2023, and shares traded at about 27 times earnings. Obviously the \$18 million CHIPS Act grant is tiny compared to the financial capability of Atlas Copco. Edwards Vacuum manufactures dry vacuum pumps elsewhere in the world, but no other domestic US producer is reported. The question is whether the firm would have proceeded with the project announced in 2022 without the CHIPS Act grant of \$18 million.

In this report's view, the grant was probably too small to have been decisive for a parent firm the size of Atlas Copco.

Project 19. Wolfspeed

On October 15, 2024, the Department of Commerce and Wolfspeed signed a nonbinding PMT to provide a **\$750 million** grant to manufacture silicon carbide chips in two locations: a new fab in Siler City, North Carolina, and support for a planned expansion in Marcy, New York. No concessional loan was announced. Previously, Wolfspeed announced a \$6 billion capital expansion plan, but the CHIPS Act announcement did not specify the amount of incremental capex triggered by the grant. This report assumes that the entire \$6 billion is tied to the grant. The implied investment tax credit subsidy at 25 percent of \$6 billion is \$1.5 billion. The two projects are forecast to create 3,000 construction jobs and 2,000 permanent manufacturing jobs.

Wolfspeed is the world's leading manufacturer of silicon carbide chips. Silicon carbide has favorable chemical and physical properties compared to traditional silicon, making the chips energy efficient and durable. They are widely used in electric and hybrid vehicles and military applications.

Wolfspeed reported revenue of \$807 million for fiscal 2024 (ending June 30), an operating loss of \$191 million, and negative earnings of \$574 million before extraordinary items. The market capitalization of equity shares in October 2024 was \$2 billion. Judging from its weak financial position, Wolfspeed would not have undertaken the new Siler City fab, nor expansion of the Marcy facility, without the CHIPS Act grant. Because Wolfspeed is the dominant producer of silicon carbide chips, an alternative US supplier (without CHIPS Act support) seems unlikely.

In this report's view, the CHIPS Act grant might have been essential to expand US production of silicon carbide chips.

Project 20. Infinera

On October 17, 2024, the Department of Commerce and Infinera signed a nonbinding PMT to provide a **\$93 million** grant to support the construction of a new fab that makes optical semiconductors in San Jose, California, and a new advanced test and packaging facility in Bethlehem, Pennsylvania. The new fab will produce indium phosphide-based photonic integrated circuits that use light to transfer information. No concessional loan was announced, and the amount of planned capex was not disclosed. The two facilities will create 1,200 construction jobs and 500 permanent manufacturing jobs. Based on the forecast number of construction jobs and the size of the grant, this report assumes that capex will total \$1 billion, implying an investment tax credit subsidy of \$250 million.

Infinera reported 2023 sales of \$1.6 billion and operating income of \$81 million. Earnings were a negative \$25 million. Market capitalization of equity was \$1.6 billion in October 2024. Because of Infinera's limited financial capacity, it seems unlikely that the firm would have committed to the two new facilities without CHIPS Act support. While Infinera is not the only domestic firm to make and package optical semiconductors, other potential suppliers would very likely require CHIPS Act funds to expand production.

In this report's view, CHIPS Act support might have been essential to expand US production of optical semiconductors.

Summary evaluation

This report cannot determine whether the CHIPS Act grants, loans, and investment tax credits were essential for each of the 20 award firms to invest at committed levels in US fabs and ATP plants. But in this report's view, the cash subsidies might have been essential for 10 out of the 20 firms.

CHIPS Act grants plus the subsidy value of concessional loans to the aforementioned 10 firms amount to \$31.4 billion. They have captured the lion's share of total CHIPS Act grants and subsidized loans so far awarded (\$38.5 billion). They will also receive \$68.6 billion subsidies from the 25 percent investment tax credits on their projected capex.

That means up to \$7.1 billion in subsidized grants and loans might have been unnecessarily awarded to 10 financially strong companies. These companies might have been driven mainly by the tax credits to make their investment commitments.

Table 11 summarizes the corporate characteristics of firms awarded CHIPS Act cash grants (panel a) and the project characteristics of each award (panel b). Whereas cash grants have been preliminarily awarded to several small firms, the biggest subsidies are going to seven giant firms: GlobalFoundries, Intel, TSMC, Samsung, Micron, SK Hynix, and Texas Instruments. Smaller firms often appear to have been awarded CHIPS Act funding not so much because they are essential suppliers on US territory but rather to achieve geographic diversity and to forestall complaints that the CHIPS Act only benefits big firms.

Table 12 summarizes the political characteristics of states where CHIPS Act projects are located. Most of the states voted Democratic in the 2020 presidential election, and most have congressional delegations that skew Democratic. However, large CHIPS Act projects are located in four Republican states—Ohio, Texas, Idaho, and Indiana—plus Arizona, which is politically divided. Based on this record, it is hard to discern a strong pro-Democratic political bias in CHIPS Act awards. However, more sophisticated statistical analysis might uncover a bias.²⁷

Question 2: Will the CHIPS Act enhance US economic and national security?

Answer: Yes, if more production equates to better security, but more production might not provide the best security for the money.

Based on our answer to the first question, it appears almost certain that the CHIPS Act will increase the manufacture of semiconductors on US territory beyond what market forces would have ensured. Industrial policy advocates are aware that US chip firms are world leaders in semiconductor design, exemplified by Qualcomm, Broadcom, and Nvidia, drawing on huge R&D outlays. But

²⁷ Cullen Hendrix suggests that normalizing new CHIPS Act jobs in a state by the number of existing semiconductor jobs in that state might reveal a tendency to use awards to bolster existing clusters and possibly a political bias that cannot be explained by existing clusters. The Department of Commerce's *Vision for Success* extols clusters as a way to accelerate technology.

advocates see a weak “lab to fab” connection: pathbreaking design by US-headquartered firms does not, through market forces, ensure manufacturing capability on US territory.

Yet domestic production is viewed as essential for economic and national security. Foremost in the security equation, US chip production decreases reliance on East Asia. Supplies from Japan, South Korea, and Taiwan are all susceptible to disruption from severe earthquakes, pandemics, and geopolitical hostilities, and Chinese chips are susceptible to outright export bans.²⁸ The CHIPS Act addresses those vulnerabilities. But since economic and national security risks arise from a wide range of threats, the question remains whether the CHIPS Act was a superior use of public money.

Economic and national security are plastic terms, frustrating for academic scholars to pin down. As Daniel Drezner has [written](#), following the onset of the cold war between the United States and China, national security has become everything, with little national consensus as to priorities. For the semiconductor industry, three US institutions largely decide which economic and national security threats deserve priority: the president, Congress, and—once the first two have provided guidance—the Department of Commerce. Without investigating other ways of spending public money to mitigate alternative threats—such as the possible loss of US chip design superiority, extreme reliance on ASML (the lithography champion), cyberattacks against US financial centers, or Chinese control of critical minerals—the president and Congress committed almost \$200 billion to boost US chip production. Nor did Congress debate alternative means of ensuring adequate chips for defense and commercial purposes, such as incentives to build inventories or to construct fabs in secure allies, such as Canada. Quite possibly, the expenditure of \$200 billion to mitigate alternative risks, or to support alternative means of guarding against chip shortages, would have been inferior strategies to the construction of chip plants on US territory. Yet, in the absence of published analysis by the White House, congressional committees, or a qualified organization such as RAND, it is hard to support that assertion.

The CHIPS Act tasks the Department of Commerce with awarding grants and concessional loans among competing applicants. Spadework is done by the department’s CPO, which recruited 150 semiconductor and financial professionals. Awards have now been given to 20 firms and, as of August 2024, nearly [\\$32 billion](#) of the appropriated \$39 billion grant and concessional loan subsidy funds have been committed (subject to performance conditions). A year earlier, in August 2023, some [460 firms](#) had expressed an interest in CHIPS Act awards. Clearly, CPO’s analysis led to the rejection of a great many applicants.

The Department of Commerce published a guidebook, [Approach to National Security](#), which spells out considerations that inform CPO analysis of project proposals. For example, does the firm have the technical capacity to produce advanced logic chips? Will it serve multiple customers, not just the US government? Will the chips fill a gap in existing US production capacity? How important are the chips to designated [critical infrastructure industries](#)?

28 China has already [limited exports](#) of two semiconductor ingredients, germanium and gallium, driving their prices much higher and hobbling production of advanced chips.

Table 11

Features of projects awarded CHIPS Act funds

a. Corporate characteristics, end of fiscal year 2023 (billions of current US dollars, except P/E ratios and bond ratings)

Company	Revenue	Income before depreciation and amortization	Income after depreciation and amortization	Market capitalization	P/E ratio	Moody's rating
BAE Systems	28.7	3.9	2.9	42.8	17.7x	Baa2
Microchip Technology	8.4	4.1	3.1	45.9	22.2x	Baa2
GlobalFoundries	7.4	2.6	1.1	33.5	23.8x	n.a.
Intel	54.2	9.7	0.1	211.9	128.9x	A2
TSMC	70.6	47.5	30.1	500.9	17.2x	Aa3
Samsung	194.2	34.8	5.1	401.3	16.8x	Aa2
Micron	15.5	2.1	-5.7	76.6	-26.3x	Baa3
Polar	n.a.	n.a.	n.a.	0.3	n.a.	n.a.
Absolics (SKC)	4.0	-0.1	-0.2	2.2	-9.4x	n.a.
Rocket Lab	0.2	-0.1	-0.2	2.7	-15.9x	n.a.
Entegris	3.5	0.9	0.5	18.0	89.9x	Ba1
Rogue Valley Microdevices	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.
GlobalWafers	2.2	1.0	0.8	8.3	12.1x	n.a.
Amkor	6.5	1.1	0.5	8.2	20.1x	Ba3
SK Hynix	21.3	1.8	-4.9	75.1	-8.5x	Baa2
Texas Instruments	17.5	9.0	7.8	154.8	21.9x	Aa3
HP	53.7	4.3	3.5	26.0	11.5x	Baa2
Edwards Vacuum (Atlas Copco)	17.2	4.6	3.7	80.1	27.0x	n.a.
Wolfspeed	0.8	-0.2	-0.6	2.0	-2.7x	n.a.
Infinera	1.6	0.1	0.0	1.1	-232.9x	n.a.

b. Project characteristics, all financial values in millions of current US dollars

Company	Location	Cash grants	Subsidy in concessional loans	Concessional loan amount	Expected tax credits	Projected capital outlays	Type of chips	Projected project benefit	Construction jobs created	Permanent jobs created
BAE Systems	Nashua, NH	35	0	0	n.a.	n.a.	Mature-node	Modernization	n.a.	30
Microchip Technology	Colorado Springs, CO	90	0	0	220	880	Mature-node	Triple the output	700	
	Gresham, OR	72	0	0	200	800	Mature-node			
GlobalFoundries	Malta, NY	1,375	128	1,600	2,900	11,600	Current-generation, mature-node	Triple the output	9,000	1,500
	Essex Junction, VT	125	0	0	225	900	Mature-node	Modernization		
	Hillsboro, OR				9,000	36,000	Leading-edge	Modernization, expansion	4,000	3,000
Intel	Chandler, AZ				8,000	32,000	Leading-edge	2 new fabs, 1 modernization	6,000	3,000
	Rio Rancho, NM	8,500	880	11,000	1,000	4,000	Advanced packaging	2 modernizations	3,000	700
	New Albany, OH				7,000	28,000	Leading-edge	2 new fabs	7,000	3,000
TSMC	Phoenix, AZ	6,600	400	5,000	16,250	65,000	Leading-edge	3 new fabs	20,000	6,000
Samsung	Taylor, TX	6,400	0	0	11,250	45,000	Leading-edge and advanced packaging	2 new leading-edge logic fabs, 1 R&D fab, and 1 advanced packaging facility	17,000	4,500
	Austin, TX							1 expansion		

b. Project characteristics, all financial values in millions of current US dollars

Company	Location	Cash grants	Subsidy in concessional loans	Concessional loan amount	Expected tax credits	Projected capital outlays	Type of chips	Projected project benefit	Construction jobs created	Permanent jobs created
Micron	Clay, NY	6,140	600	7,500	12,500	100,000	Leading-edge	2 new fabs	4,500	9,000
	Boise, ID					25,000	Leading-edge	1 new fab	4,500	2,000
Polar	Bloomington, MN	120	0	0	131	525	Mature-node	Double the output of sensor and power chips	160	
Absolics	Covington, GA	75	0	0	125	500	Materials for advanced packaging	n.a.	1,000	200
Rocket Lab	Albuquerque, NM	24	0	0	38	150	Mature-node	Modernization, expansion, increase compound semiconductor production by 50 percent within the next 3 years	n.a.	100
Entegris	Colorado Springs, CO	75	0	0	150	600	Equipment and materials	New facility	500	600
Rogue Valley Microdevices	Palm Bay, FL	6.7	0	0	6.25	25	Mature-node	New facility, triple its current manufacturing capacity	n.a.	75
GlobalWafers	Sherman, TX	400	0	0	1,000	4,000	Wafers	New facility, expansion	1,700	880
	St. Peters, MO						Wafers	New facility		
Amkor Technology	Peoria, AZ	400	16	200	500	2,000	Advanced packaging and testing	New facility	n.a.	2,000

b. Project characteristics, all financial values in millions of current US dollars

Company	Location	Cash grants	Subsidy in concessional loans	Concessional loan amount	Expected tax credits	Projected capital outlays	Type of chips	Projected project benefit	Construction jobs created	Permanent jobs created
SK Hynix	West Lafayette, IN	450	40	500	968	3,870	Packaging	New facility	1,000	
Texas Instruments	Sherman, TX	1,600	240	3,000	4,500	18,000	Current-generation, mature-node	2 new fabs	9,500	2,000
	Lehi, UT							1 new fab		
HP	Corvallis, OR	50	0	0	n.a.	n.a.	Mature-node	Expansion, modernization	150	100
Edwards Vacuum	Basom, NY	18	0	0	80	319	Dry vacuum pumps	New facility	n.a.	600
Wolfspeed	Siler City, NC	750	0	0	1,500	6,000	Silicon carbide	1 new fab	3,000	2,000
	Marcy, NY							Fab expansion		
Infirera	San Jose, CA	93	0	0	250	1,000	Indium phosphide photonics	1 new fab, increase production capacity by a factor of 10	1,200	500
	Bethlehem, PA							Assembly, testing, and packaging		

n.a. = not available; P/E ratio = price-earnings ratio; R&D = research and development

Notes: In panel a, the fiscal year of Microchip Technology ends on March 31, Micron's fiscal year ends on August 31, and the fiscal year of HP ends on October 31. Other public company fiscal years end on December 30 or 31. For a few small private companies, the financials of parent companies (mentioned in parentheses) are reported in the table. In panel b, the subsidy in concessional loans is estimated at 8 percent of the loan amount. Expected tax credits are estimated based on 25 percent of projected total capital outlays, except for Intel and Micron, for which only projected capital outlays in the next six years are used to estimate the tax credits.

Sources: Zacks (<https://www.zacks.com/>); Finbox (<https://finbox.com/>); Moody's (<https://www.moody.com/>); Semiconductor Industry Association (<https://www.semiconductors.org/>); National Institute of Standards and Technology (<https://www.nist.gov/>); US Department of Commerce (<https://www.commerce.gov/>); Intel (<https://www.intel.com/>); Taiwan Semiconductor Manufacturing Company (<https://www.tsmc.com/english>).

Table 12

Political character of states awarded CHIPS Act projects

Company	Location	State voting record in 2020 presidential election	State congressional delegation by party, Democrats to Republicans, 2022
BAE Systems	Nashua, NH	Democratic	4-0
Microchip Technology	Colorado Springs, CO	Democratic	7-3
	Gresham, OR	Democratic	6-2
GlobalFoundries	Malta, NY	Democratic	17-11
	Essex Junction, VT	Democratic	3-0
Intel	Hillsboro, OR	Democratic	6-2
	Chandler, AZ	Democratic	5-6
	Rio Rancho, NM	Democratic	5-0
	New Albany, OH	Republican	6-11
TSMC	Phoenix, AZ	Democratic	5-6
Samsung	Taylor, TX	Republican	13-27
	Austin, TX		
Micron	Clay, NY	Democratic	17-11
	Boise, ID	Republican	0-4
Polar	Bloomington, MN	Democratic	6-4
Absolics	Covington, GA	Democratic	7-9
Rocket Lab	Albuquerque, NM	Democratic	5-0
Entegris	Colorado Springs, CO	Democratic	7-3
Rogue Valley Microdevices	Palm Bay, FL	Republican	8-22
GlobalWafers	Sherman, TX	Republican	13-27
	St. Peters, MO	Republican	2-8
Amkor Technology	Peoria, AZ	Democratic	5-6
SK Hynix	West Lafayette, IN	Republican	2-9
Texas Instruments	Sherman, TX	Republican	13-27
	Lehi, UT	Republican	0-6
HP	Corvallis, OR	Democratic	6-2
Edwards Vacuum	Basom, NY	Democratic	17-11
Wolfspeed	Siler City, NC	Republican	7-9
	Marcy, NY	Democratic	17-11
Infinera	San Jose, CA	Democratic	42-12
	Bethlehem, PA	Democratic	11-8

Source: CNN (<https://edition.cnn.com/election/2020/results/president/>); Ballotpedia (https://ballotpedia.org/Election_results,_2022:_Comparison_of_state_delegations_to_the_117th_and_118th_Congresses).

Another Department of Commerce publication, *Vision for Success*, enumerates three metrics: strengthening supply chain resilience so the United States is not caught short by the interruption of critical components, advancing technological leadership by attracting frontier foreign firms (e.g., TSMC, Samsung, SK Hynix) to build US plants, and supporting vibrant fab clusters to nourish firm-to-firm learning. Nonetheless, CHIP Act grants are generally limited to 15 percent of capital costs, making other funding sources essential (the investment tax credit is an important source). Whatever the security merits of a project, it will not be totally funded by public money. It must have the prospect of commercial success.

Since the applications and CPO analysis are confidential, external reviewers, such as the authors of this report, cannot say whether the failure to meet economic and national security interests was a deciding factor for most of the rejections. Perhaps a great many applicants met the CPO's security criteria. And perhaps technological proficiency or commercial prospects then became the deciding factors. The largest awards were evidently made to established producers of advanced and leading-edge chips, including three Asian firms: TSMC, Samsung, and SK Hynix. If Congress is curious about the weight given to economic and national security interests in making awards, it should call on the Department of Commerce for a confidential report covering at least three aspects of the selection process: how many applicants were rejected on security criteria, what features made the difference between winners and runners-up, and what conditions are imposed on winners to ensure continued observance of US security interests.

The 25 percent investment tax credit, arguably the largest CHIPS Act subsidy, is not conditioned on an analysis of security interests. Congress evidently decided that greater domestic semiconductor production enhances US security, without further inquiry into the types of chips delivered by market forces. If an extended investment tax credit sparks congressional debate prior to its expiration in January 2027, the security contribution made by projects rewarded by the Department of Commerce should be contrasted with projects solely inspired by the 25 percent tax credit.

Question 3: Will the CHIPS Act reduce US dependence on imported chips?

Answer: This report is skeptical.

Bilateral and world trade flows illuminate national strengths and weaknesses as reflected in production costs. For most countries, readily available semiconductor trade figures are reported in the [UN Comtrade Database](#) under 6-digit Harmonized System (HS) trade codes that correspond to North American Industry Classification System (NAICS) code 334413. Table 13 shows the relevant HS codes. For US exports and imports of semiconductors, the US Census Bureau publishes more detailed 10-digit HS codes under each 6-digit HS code (the 6-digit and 10-digit codes differ slightly as between imports and exports).

Table 13 shows detailed 10-digit codes and, for each code, the unit value of exports and imports in three different years (2014, 2019, and 2023). Each 10-digit code reports granular data on individual chips. For most codes, the quantity unit is number of chips ("no."), but for some it is weight ("kg"). As table 13 shows, unit values for US exports almost always exceed unit values for imports in each 10-digit code that reports number of chips. In other words, within each 10-digit

Table 13

Unit values for US semiconductor exports and imports, by 10-digit HS code

Harmonized System (HS) code	Commodity	2014		2019		2023	
		Exports	Imports	Exports	Imports	Exports	Imports
381800	Chemical Elements Doped, Used In Electronics, Discs, Wafers Etc.						
3818000000	Chemical elements doped for use in electronics, in the form of discs, wafers, or similar forms; chemical compounds doped for use in electronics (kg)	155.08		379.38		392.64	
3818000010	Gallium arsenide wafers, doped (kg)		600.08		632.24		827.98
3818000090	Other chemical elements doped for use in electronics, discs, wafers, etc. (kg)		560.08		570.16		556.38
852352	Smart Cards						
8523520010	Smart cards, unrecorded (no.)	0.56	0.19	0.51	0.18	0.83	0.09
8523520090	Smart cards, recorded (no.)	2.07	0.79	2.54	0.47	2.73	0.34
854110	Diodes Except Photosensitive Or Light-Emitting Diodes						
8541100040	Chips and wafers for diodes except photosensitive (no.)	0.58	0.27	0.72	0.29	0.98	0.39
8541100050	Zener diodes (no.)	0.07	0.03	0.09	0.03	0.10	0.03
8541100060	Microwave diodes (no.)	4.22	0.12	6.39	0.24	5.66	0.40
8541100070	Semiconductor diodes not photosensitive, less than or equal to 0.5 A (no.)	0.13	0.01	0.10	0.01	0.17	0.01
8541100080	Semiconductor diodes not photosensitive, greater than 0.5 A (no.)	0.08	0.05	0.10	0.05	0.14	0.06
854121	Transistors Except Photosensitive, Dissipation Rate Less than 1 W						
8541210040	Chips, dice and wafers, transistors other than photosensitive (no.)	0.25	0.39	0.18	0.26	0.45	0.33
8541210075	Transistors with dissipation rate less than 1 W, frequency greater than or equal to 100 MHz (no.)		0.02		0.02		0.03
8541210080	Transistors other than photosensitive, less than 1 W, nesoi (no.)	0.40		0.53		0.56	
8541210095	Transistors with dissipation rate less than 1 W, frequency less than 100 MHz (no.)		0.02		0.02		0.03
854129	Transistors, Other Than Photosensitive, Nesoi						
8541290040	Transistor chips other than photosensitive, greater than or equal to 1 W (no.)	3.01	0.57	4.13	0.43	7.30	1.35
8541290075	Transistors, except photosensitive, greater than 1 W, frequency greater than 30 MHz (no.)		0.23		0.41		1.00

Harmonized System (HS) code	Commodity	2014		2019		2023	
		Exports	Imports	Exports	Imports	Exports	Imports
8541290080	Transistors other than photosensitive, greater than or equal to 1 W (no.)	0.67		0.75		0.73	
8541290095	Transistors, except photosensitive, greater than 1 W, frequency less than 30 MHz (no.)		0.23		0.24		0.39
854130	Thyristors, Diacs and Triacs, Except Photosensitive Devices						
8541300040	Chips for thyristors, diacs, and triacs (no.)	2.11	0.24	0.88	0.26	3.86	0.45
8541300080	Thyristors, diacs, and triacs, not photosensitive, nesoi (no.)	2.05	0.56	3.26	0.55	1.83	0.76
854140	Photosensitive Semiconductor Devices Including Photovoltaic Cells Etc.						
8541402000	Light-emitting diodes (LEDs) (no.)	0.12	0.19	0.14	0.11	0.19	0.10
8541406010	Chips and wafers for photosensitive diodes (no.)	6.81	0.84	3.37	2.82	4.69	2.65
8541406020	Solar cells assembled into modules or panels (no.)	253.40	75.04	586.82	95.76	540.78	99.79
8541406025	Solar cells, crystalline silicon photovoltaic cells, nesoi (no.)				1.75		1.18
8541406030	Solar cells, not made into panels or modules (no.)	60.21	2.18	53.56		61.11	
8541406035	Solar cells, made into panels or modules, nesoi (no.)				78.97		99.85
8541406045	Solar cells, nesoi (no.)				6.68		5.22
8541406050	Photosensitive diodes, nesoi (no.)	8.17	2.07	8.16	2.08	9.77	2.53
8541407040	Chips and wafers for photosensitive transistors (no.)	38.84	1.49	0.26	0.36	0.19	0.54
8541407080	Photosensitive transistors, nesoi (no.)	0.77	0.34	1.22	0.52	1.39	0.39
8541408000	Optical coupled isolators (no.)	3.94	0.64	3.85	1.02	3.52	0.85
8541409500	Photosensitive semiconductor devices, nesoi (no.)	35.15	2.52	34.97	2.49	26.13	2.08
854150	Semiconductor Devices Except Photosensitive/Photovoltaic Cells						
8541500040	Chips and wafers for semiconductor devices, nesoi (no.)	9.39	3.65	11.86	1.75	11.26	2.92
8541500080	Semiconductor devices, nesoi (no.)	2.87	1.47	4.15	1.46	3.20	1.84
854190	Parts for Diodes, Transistors and Similar Semiconductors						
8541900000	Diodes, transistors, and similar semiconductor device parts (no.)					1.18	1.04
854231	Processors and Controllers, Electronic Integrated Circuits						
8542310000	Processors and controllers whether or not combined with memories, etc. (no.)	15.68	5.49	9.47	8.46	9.91	7.73

Harmonized System (HS) code	Commodity	2014		2019		2023	
		Exports	Imports	Exports	Imports	Exports	Imports
854232	Memories, Electronic Integrated Circuits						
8542320001	Dynamic read-write random access memory (DRAM), less than or equal to 128 megabits (Mb) (no.)		1.02		2.69		3.18
8542320015	Electric integrated circuits memory, DRAM, not over 1 gigabit (Gb) (no.)	1.66		0.95		1.69	
8542320020	DRAM greater than 128 Mb, less than or equal to 256 Mb (no.)		2.19				
8542320021	DRAM greater than 256 Mb, less than or equal to 512 Mb (no.)		3.18				
8542320022	DRAM greater than 512 Mb, less than or equal to 1 Gb (no.)		2.25				
8542320023	DRAM over 1Gb (no.)	4.45	3.37	1.80	4.81	1.35	5.12
8542320024	DRAM greater than 128 Mb, less than or equal to 256 Mb (no.)				2.61		2.71
8542320028	DRAM greater than 256 Mb, less than 512 Mb (no.)				2.80		5.12
8542320032	DRAM greater than 512 Mb, less than or equal to 1 Gb (no.)				2.54		5.92
8542320040	Static read-write random access memory (SRAM) (no.)	9.94	3.01	7.54	4.64	9.54	3.38
8542320050	Electrically erasable programmable read-only memory (EEPROM) (no.)	2.57	1.21	1.63	1.74	0.76	0.53
8542320060	Erasable (except electrically) programmable read-only memory (EPROM) (no.)	2.61	2.09	9.08	2.02	6.39	2.54
8542320070	Electric integrated circuits, memory, nesoi (no.)	4.44	1.43	5.58	2.15	5.00	1.64
854233	Amplifiers, Electronic Integrated Circuits						
8542330000	Electronic integrated circuits, amplifiers (no.)	0.81	0.44	1.30	0.61	1.23	0.92
854239	Electronic Integrated Circuits, Nesoi						
8542390000	Electronic integrated circuits, nesoi (no.)	3.30	0.82	3.13	0.90	3.06	1.23
854290	Electronic Integrated Circuits and Microassemblies						
8542900000	Electronic integrated circuits and microassembly parts (no.)					1.29	2.50

kg = kilogram; MHz = megahertz; no. = number of chips; W = watt; nesoi = not elsewhere specified or included

Notes: The missing export and import unit values of the 10-digit HS code commodities under "854140 Photosensitive semiconductor devices, including photovoltaic cells, etc." and "854150 Semiconductor devices, except photosensitive/ photovoltaic cells" in 2023 are filled with the unit values in 2021. Some export and import commodities having different 10-digit HS codes are combined based on commodity descriptions.

Source: US Census Bureau (<https://www.census.gov/>).

code, US exports apparently have superior characteristics—meaning they are more advanced—than US imports.

This finding startles some observers since a strong motivation for the CHIPS Act is the absence of US foundries that produce advanced logic chips. How can the United States export relatively high-value chips when it depends on imports for advanced logic chips? The explanation seems to hinge on the pure-play foundries centered in Taiwan and South Korea. The foundries fulfill detailed contracts to export specified chips to US design firms. In turn, the firms retail the chips at very high markups to reflect intellectual property embodied in proprietary designs.

Table 14 summarizes the dollar value of US and other Big 6 semiconductor trade for the 10-year period 2014–23. The table is divided into four panels. Panel a summarizes the annual dollar value of US chip exports and imports with other Big 6 jurisdictions and the world. For most flows, US bilateral trade with other Big 6 jurisdictions falls in the low billion-dollar range. With Japan and Korea, the value of US two-way chip trade in 2023 is not much different than 2014, despite the rapid growth in global industry sales. For geopolitical reasons, US two-way chip trade with China dropped sharply in 2023. Only with the European Union and Taiwan has two-way trade grown significantly, approximately doubling with both partners. Meanwhile, the value of US two-way chip trade with the rest of the world (ROW) has grown at a modest rate, rising from around \$50 billion in 2014 to over \$60 billion in 2023.

In terms of trade balances, both for individual Big 6 jurisdictions and for the ROW, exports and imports are closely balanced. Large surpluses or deficits are unusual. The data suggest approximate overall equivalence in competitive strength between US and foreign producers. As shown later, on a granular basis, the United States is stronger for advanced chips and weaker for mature chips.

What should we expect from overall trade flows once the CHIPS Act fabs enter into production? If anything, US imports should continue to be sluggish as domestic production replaces imports. However, there is less reason to expect an export surge since US production costs at the new fabs will likely exceed production costs from East Asia. Moreover, most of the new production from firms receiving CHIPS Act awards will be purchased by US industrial users.

Panel b of table 14 takes a different look at trade. The focus is on unit values of 10-digit US exports and imports to different destinations during the years 2014–23, covering only those 10-digit codes quantified as number of items—meaning that codes expressed as kilograms are excluded because individual chips weigh far less than a kilogram. Panel b reports the percentage by value of US exports and imports to each destination that can be characterized as “advanced chips”—using unit values to define *advanced*. To be clear, this is a different way of defining *advanced* than the metrics used for CHIPS Act grants.

Unit values in the semiconductor trade space are widely dispersed—ranging from under \$1 to over \$1,000—and quantities expressed as number of items are heavily skewed toward lower-valued chips. Thus, panel b reports the dollar value of exports and imports for which the natural logarithms of unit values exceed a defined threshold. The intuition of panel b is that larger unit value logarithms denote more advanced chips. Using an arbitrary cutoff at natural logarithms of 2 and larger, the data in panel b indicate the percentage (by value) of exports and imports that meet or exceed the threshold. These are characterized as “advanced

Table 14

Semiconductor trade in the Big 6 jurisdictions, 2014-23

<i>a. Semiconductor trade between the United States and the other Big 6 jurisdictions (billions of current US dollars)</i>										
Item	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
US exports to China	5.5	6.0	6.0	6.2	7.1	9.0	11.2	13.4	10.5	6.3
US imports from China	4.9	5.3	5.4	5.0	4.8	2.6	2.8	3.2	3.9	2.9
US balance with China	0.6	0.6	0.6	1.1	2.3	6.4	8.5	10.2	6.6	3.4
US exports to EU	2.2	2.1	2.2	2.8	3.3	4.1	4.6	5.6	6.1	5.4
US imports from EU	1.9	2.2	4.4	4.0	2.9	2.6	2.2	3.9	4.9	4.5
US balance with EU	0.3	-0.1	-2.2	-1.2	0.4	1.4	2.5	1.7	1.1	0.9
US exports to Japan	1.1	1.1	1.2	1.0	1.2	1.0	1.0	1.3	1.4	1.1
US imports from Japan	3.2	3.1	2.9	2.9	3.1	2.8	2.5	2.7	2.9	2.7
US balance with Japan	-2.1	-2.0	-1.8	-1.8	-1.9	-1.8	-1.5	-1.4	-1.6	-1.6
US exports to Korea	3.7	3.6	2.9	3.4	3.4	3.3	3.2	2.9	2.4	2.6
US imports from Korea	2.8	2.8	3.3	3.3	3.2	3.2	3.4	3.7	4.4	3.6
US balance with Korea	0.9	0.7	-0.4	0.0	0.3	0.1	-0.2	-0.8	-2.0	-0.9
US exports to Taiwan	2.9	3.3	3.8	3.7	3.6	3.4	3.9	5.1	6.0	5.3
US imports from Taiwan	5.1	4.5	4.2	4.4	4.8	4.3	4.3	6.2	9.1	8.2
US balance with Taiwan	-2.2	-1.2	-0.4	-0.8	-1.2	-0.9	-0.4	-1.1	-3.1	-2.8
US exports to rest of world	27.3	25.8	26.8	29.1	27.9	29.7	29.7	33.4	34.8	32.4
US imports from rest of world	22.4	23.7	25.3	25.8	26.6	29.7	31.1	36.3	34.5	29.5
US balance with rest of world	4.9	2.0	1.4	3.3	1.3	0.0	-1.4	-3.0	0.3	2.9
Total US exports to world	42.7	41.8	42.8	46.2	46.5	50.5	53.7	61.7	61.2	53.2
Total US imports from world	40.4	41.7	45.5	45.4	45.3	45.3	46.2	56.0	59.8	51.4
Total US balance with world	2.4	0.1	-2.8	0.7	1.2	5.2	7.6	5.7	1.4	1.8

<i>b. Share of US export and import bilateral trade values characterized as "advanced chips" (percent)</i>										
Item	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
US exports to China	55.1	67.9	72.1	57.8	65.5	78.7	79.1	77.7	68.4	52.2
US imports from China	35.1	35.0	30.1	14.7	3.2	7.1	15.8	0.9	0.8	1.1
Percent difference with China	20.0	32.9	42.0	43.0	62.3	71.5	63.2	76.7	67.7	51.1
US exports to EU	46.0	47.2	51.2	55.8	52.9	64.4	70.0	61.6	52.2	57.0
US imports from EU	19.4	33.4	81.8	79.3	18.0	15.0	24.3	65.7	66.7	65.7
Percent difference with EU	26.6	13.8	-30.6	-23.5	34.9	49.3	45.7	-4.1	-14.5	-8.7
US exports to Japan	51.5	83.3	24.1	24.4	23.9	40.2	38.1	24.7	30.3	41.0
US imports from Japan	17.1	17.4	17.1	16.7	18.7	19.6	22.3	6.7	9.9	14.9
Percent difference with Japan	34.5	65.9	7.0	7.7	5.2	20.5	15.7	18.0	20.4	26.0

b. Share of US export and import bilateral trade values characterized as “advanced chips” (percent)

Item	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
US exports to Korea	72.0	79.9	75.2	79.4	79.4	91.3	81.2	79.2	68.3	77.0
US imports from Korea	70.1	75.5	80.3	78.6	75.7	60.8	24.0	31.9	88.5	79.6
Percent difference with Korea	2.0	4.4	-5.1	0.9	3.6	30.6	57.2	47.3	-20.3	-2.6
US exports to Taiwan	27.2	29.4	44.6	39.6	57.5	41.9	46.0	36.4	34.1	36.1
US imports from Taiwan	15.4	7.8	5.6	1.1	9.7	2.3	1.9	6.0	0.5	0.5
Percent difference with Taiwan	11.8	21.6	39.0	38.5	47.8	39.6	44.1	30.4	33.7	35.6
Total US exports to world	49.5	51.6	7.4	4.7	6.4	59.2	61.3	58.3	52.7	52.1
Total US imports from world	12.1	16.3	19.7	13.0	8.5	63.2	66.5	63.6	54.5	53.0
Percent difference with world	37.4	35.3	-12.3	-8.4	-2.1	-4.0	-5.2	-5.2	-1.7	-1.0

c. Share of US export and import bilateral trade values characterized as “highly advanced chips” (percent)

Item	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
US exports to China	2.3	1.6	1.8	2.1	1.7	3.3	2.8	1.9	2.4	7.6
US imports from China	35.1	35.0	30.1	14.7	3.2	7.0	12.3	0.9	0.7	1.0
Percent difference with China	-32.8	-33.3	-28.3	-12.7	-1.4	-3.8	-9.5	1.0	1.6	6.6
US exports to EU	44.9	44.4	12.5	17.3	11.2	7.1	5.3	60.0	48.5	50.1
US imports from EU	10.1	31.1	6.0	9.0	12.2	10.9	18.3	8.6	6.7	7.5
Percent difference with EU	34.7	13.4	6.5	8.2	-0.9	-3.8	-13.0	51.4	41.7	42.6
US exports to Japan	49.1	22.3	22.4	21.3	20.8	20.9	29.5	10.1	14.1	22.7
US imports from Japan	8.1	11.4	15.3	9.5	11.6	8.7	14.8	1.0	1.0	1.0
Percent difference with Japan	41.0	10.9	7.2	11.8	9.2	12.2	14.7	9.0	13.1	21.7
US exports to Korea	71.8	79.8	74.5	77.1	77.3	78.4	79.2	76.3	64.9	74.0
US imports from Korea	4.6	23.4	40.3	33.9	20.8	15.7	21.5	18.0	14.9	14.6
Percent difference with Korea	67.2	56.4	34.3	43.2	56.5	62.6	57.6	58.3	50.1	59.4
US exports to Taiwan	24.8	28.8	1.8	4.9	35.5	38.1	38.6	35.7	33.4	35.4
US imports from Taiwan	15.4	7.8	5.6	1.0	0.9	2.3	1.4	0.7	0.5	0.5
Percent difference with Taiwan	9.4	21.0	-3.8	4.0	34.5	35.8	37.2	35.0	32.9	34.9
Total US exports to world	4.6	4.5	4.6	4.3	4.1	3.8	0.5	0.5	0.5	0.6
Total US imports from world	12.1	16.3	19.7	12.7	8.3	14.4	18.2	11.6	10.9	12.6
Percent difference with world	-7.5	-11.7	-15.0	-8.4	-4.2	-10.6	-17.7	-11.1	-10.4	-12.1

d. Semiconductor trade between the other Big 6 jurisdictions and the world (billions of current US dollars)

Item	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
Total Chinese exports to world	94.4	104.0	91.0	97.5	117.3	139.5	155.2	206.5	209.7	190.6
Total Chinese imports from world	248.4	258.8	253.5	287.7	340.5	331.9	376.7	465.2	449.6	380.1
China's balance with world	-154.0	-154.7	-162.5	-190.1	-223.2	-192.4	-221.5	-258.8	-239.9	-189.5

d. Semiconductor trade between the other Big 6 jurisdictions and the world (billions of current US dollars)

Item	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
Total EU exports to world	21.9	20.4	24.9	27.8	28.9	31.3	32.4	39.1	44.4	39.0
Total EU imports from world	30.2	29.7	29.5	38.1	45.6	46.1	46.0	62.2	75.4	70.9
EU balance with world	-8.3	-9.3	-4.6	-10.3	-16.7	-14.8	-13.5	-23.1	-31.0	-31.9
Total Japanese exports to world	35.9	33.1	33.6	36.9	39.6	38.9	40.3	47.0	47.1	43.5
Total Japanese imports from world	27.7	25.4	23.8	25.5	26.3	24.4	24.2	31.4	38.0	34.9
Japan's balance with world	8.2	7.7	9.8	11.4	13.3	14.5	16.1	15.6	9.0	8.6
Total Korean exports to world	57.4	57.9	58.6	92.9	117.0	85.3	88.6	115.3	119.0	119.0
Total Korean imports from world	35.8	37.0	35.3	39.7	41.6	42.9	47.1	58.5	70.9	70.9
Korea's balance with world	21.7	20.9	23.2	53.2	75.5	42.4	41.5	56.8	48.2	48.2
Total Taiwanese exports to world	82.9	78.9	86.7	100.2	102.7	105.8	128.5	162.9	190.1	190.1
Total Taiwanese imports from world	40.5	37.4	41.8	49.2	56.3	58.4	67.6	87.6	94.3	94.3
Taiwan's balance with world	42.4	41.5	44.9	51.1	46.4	47.4	60.9	75.3	95.8	95.8

Notes: The missing trading value of Harmonized System codes “854140 Photosensitive semiconductor devices, including photovoltaic cells, etc.” and “854150 Semiconductor devices, except photosensitive/photovoltaic cells” in 2022 and 2023 have been filled with the 2021 values in both panels a and d. In panel b, “advanced chips” are defined as chips with a natural log of the unit value greater than or equal to 2. In panel c, “highly advanced chips” are defined as chips with a natural log of the unit value greater than or equal to 3. In panels b and c, percentages are calculated based on the proportion of export and import values, and commodities reported using kilogram as a unit are excluded from the unit value analysis. In panel d, the missing total trade values of Korea and Taiwan to the world in 2023 have been filled with the 2022 values.

Sources: US Census Bureau (<https://www.census.gov/>); UN Comtrade Database (<https://comtradeplus.un.org/>).

chips.” Of course, it would be better if 10-digit HS codes were distinguished in degrees between mature and advanced semiconductors, but the Census Bureau chose different characteristics for its 10-digit HS codes. Consequently, panel b relies on unit values to make the distinction.

The percentages of US export values sent to China and Taiwan are consistently high in advanced chips, whereas the percentages of US import values arriving from China and Taiwan have trended lower in advanced chips. Likewise, US exports to Japan are generally more advanced than imports from Japan. But the distinction between exports and imports is much weaker, sometimes even reversed, for US bilateral trade with the European Union and Korea. For US two-way trade with the world between 2019 and 2023, there is not much difference between the percentage of advanced exports and advanced imports, based on unit value data.

Panel c in table 14 carries the unit value analysis of advanced chips a step further. It reports the percentage of trade value for HS 10-digit codes with log unit values of 3 or greater that were shipped to, or purchased from, one or more of the other Big 6 jurisdictions between the years 2014 and 2023. There were more than 50 such HS 10-digit codes over the entire period. As the table indicates, the percentage of trade value for US export items far exceeds the percentage of trade value for US import items.

It is worth repeating an earlier observation about the apparent disconnect between the absence of US production of advanced logic chips and large US

exports of high unit value chips. The answer appears to lie in the pure-play foundries. They ship to US design firms chips made to contractual specifications, which are then resold to US and foreign business consumers at much higher prices, reflecting the embodied value of proprietary intellectual property.

What should we expect in terms of unit value analysis once the CHIPS Act fabs are in full swing? While mature chips are the bread and butter of a few awards, the bulk of grants, loans, and tax credits are aimed at advanced fabs and ATPs. This should result in some decline in the percentage of imports characterized as advanced chips in the years ahead. But it might not lead to much increase in the percentage of advanced chips exported by the United States to other Big 6 jurisdictions. They are busy subsidizing their own production of advanced chips to reduce their dependence on the United States.

Panel d in table 14 summarizes the dollar value of semiconductor trade with the world by the other Big 6 jurisdictions. China, South Korea, and Taiwan more than doubled their exports between 2014 and 2023. Because of its large production of consumer electronics, China ran a growing trade deficit in chips, and South Korea and Taiwan both reported large chip trade surpluses throughout the period. Based on these observations, we conclude that South Korea and Taiwan have strong competitive advantages in the semiconductor sphere. Japan's trade profile over the decade roughly resembles the US profile. Neither country exhibits a strong competitive advantage or disadvantage. With persistent large deficits, both China and the European Union reveal their competitive disadvantage in semiconductor trade. This conclusion is reinforced by the fact that both China and the European Union have generally run overall merchandise trade surpluses with the world over the past decade, China to a much larger extent than the European Union. But in the chips sector, China and the European Union run trade deficits.

Although the CHIPS Act might produce surprising outcomes, this report is skeptical that subsidized foundries will give the United States a strong competitive advantage in chips. To reiterate a central feature, the CHIPS Act was not foremost designed to create a US competitive advantage in global chips trade but rather to locate a substantial share of advanced chip manufacture on US soil. While US subsidies are large, they do not appear large enough to confer on the United States the strong competitive advantages enjoyed by South Korea and Taiwan.

Question 4: Will the United States produce 20 percent of the world's advanced chips by 2030?

Answer: Maybe.

In its **NOFO**, NIST gave this definition of leading-edge facilities and the chips that they produce:

Leading-Edge Facilities for logic or memory that utilize the most advanced front-end fabrication processes which achieve the highest transistor and power performance. For logic, this currently includes facilities that produce semiconductors at high volumes using extreme ultraviolet (EUV) lithography tools. For memory, this currently includes facilities capable of producing 3D NAND flash chips with 200 layers and above, and/or dynamic random-access memory (DRAM) chips with a half-pitch of 13nm and below.

A [timely report](#) authored by BCG and SIA projects that US capex on advanced logic chips (less than 10 nm), made with EUV lithography, will increase from 0 percent of global capex before 2024 to 28 percent by 2032. This will be achieved by \$646 billion capex in US foundries, of which 30 percent (\$194 billion) will be spent by US firms, 37 percent (\$239 billion) by Korean firms (mainly Samsung and SK Hynix), 32 percent (\$207 billion) by Taiwanese firms (mainly TSMC), and 1 percent by EU firms (\$6 billion). To summarize, the forecast capex on American territory by Korean and Taiwanese firms amounts to \$446 billion between 2024 and 2032.

If the BCG and SIA projections are realized, then Secretary Raimondo's aspiration that the United States will produce 20 percent of global advanced chips in 2030 seems plausible. But are the capex projections too optimistic?

Global capex outlays on wafers, primarily for advanced logic and memory chips over the period 2024–32, are projected to reach \$2.3 trillion. Without the CHIPS Act, the BCG and SIA report estimates that only 9 percent of the global capex would have been spent in US territory—in other words, \$207 billion, rather than 28 percent, or \$646 billion. By this arithmetic, the CHIPS Act will attract \$439 billion in leading-edge capex to US territory.

How does the \$439 billion figure stack up against current US offerings of chip subsidies? Cash grants will eventually total \$39 billion, including the subsidy element of \$75 billion concessional loans is implicitly estimated by the Congressional Budget Office at \$6 billion (8 percent of loans). The biggest subsidy is the [25 percent investment tax credit](#), good for capex starting with the passage of the CHIPS Act in August 2022 and lasting through projects initiated before January 2027. Assuming, as the industry clearly hopes, that the investment tax credit will be renewed to cover all capex through 2032, the total tax credit benefit might reach \$150 billion (roughly 25 percent of \$646 billion). All told, US subsidies would then approach \$189 billion (\$39 billion plus \$150 billion) over the period 2024–32. Incentives of this magnitude would seem ample to spur additional capex of \$439 billion.

A big uncertainty is whether global demand for advanced chips will support the forecast massive investments contemplated by all Big 6 jurisdictions. Although semiconductor demand exhibits [strong cyclical characteristics](#), and thus [deep recessions](#), the long-term sales trend is strongly positive. As observed early in this report, the industry illustrates Say's law: Supply creates its own demand. In the case of semiconductors, the supply is constant technological improvement. The latest spectacular episode is the AI boom led by Nvidia. Still, two clouds must be noted: AI electricity demands are already straining the US grid, and workers with the requisite skills are in short supply.

In December 2022, a few months after the CHIPS Act was signed, SIA reported that \$200 billion of new investment had been “sparked” by anticipation of passage since May 2020, when the act was [first introduced](#) in Congress. This figure was raised to almost \$450 billion of investment projects “sparked” between May 2020 and April 2024, when the report [was updated](#). Excluding \$114 billion of investment by Asian firms (chiefly TSMC, Samsung, and SK Hynix) leaves a projection of about \$333 billion capex by US firms. That figure more than covers the projected capex by US firms in advanced logic chips between 2024 and 2032. However, announced capex by TSMC, Samsung, and SK Hynix

(all awarded CHIPS Act grants), totaling \$114 billion, falls well short of the BCG and SIA projection of \$446 billion capex on American territory by Korean and Taiwanese chip firms between 2024 and 2032.

For three reasons, it can be questioned whether the Asian chip giants will pour \$446 billion into US capex for leading-edge logic and memory chips by 2032. First, cash grants and loan subsidies (the \$39 billion fund) will be committed by 2025. Given the magnitude of US budget deficits, it is unclear whether this fund will be replenished in Trump's second presidential term (2025–29).

Second, to claim the 25 percent investment tax credit under existing law, projects must be launched before January 2027. The investment tax credit is a major incentive—exceeding the prospective benefit from cash grants—but because it is less conspicuous than cash grants, it might be extended in 2027. Again, however, US budget deficits argue against extension.

Third, and most important, the Asian chip giants in Korea and Taiwan have launched their own massive capex programs at home, spurred by generous tax credits designed to match the US offering. According to BCG and SIA projections, wafer capex in Taiwan between 2024 and 2032 is projected to reach \$716 billion, almost entirely by Taiwanese firms (dominated by TSMC), and wafer capex in Korea is projected to reach \$300 billion, entirely by Korean firms (dominated by Samsung and SK Hynix). Because chip firms are bigger players in the economic landscape of Korea and Taiwan than in the United States, current Asian incentive programs (centered on tax credits) seem more certain to be extended than the US investment tax credit. Moreover, capital and operating costs in Asia are lower than in the United States. These factors suggest that, if global chip sales flag by comparison with current projections, Asian giants are likely to pull back on US capex before they reduce home capex.

In conclusion, it seems questionable that the magnitude of Korean and Taiwanese semiconductor capex on American territory will be sufficient to meet the target of 20 percent of global capacity for advanced chips made on US soil by 2030. If 20 percent is seen by future US presidents and congressional leaders as an essential target, further subsidies beyond the CHIPS Act are probably required.

Question 5: How many jobs will be created and at what subsidy cost per job-year?

Answer: Approximately 93,000 construction jobs and 43,000 permanent jobs will be created, at an average subsidy cost of \$185,000 per job-year.

Job creation was, at best, a tertiary objective of the CHIPS Act. Nevertheless, announcements by the Department of Commerce and statements by President Biden at award ceremonies touted job numbers. The numbers have political importance, and for that reason a short assessment is relevant.

Making the strong assumption that all fabs awarded federal subsidies would not otherwise have been built, table 15 shows reported construction and permanent employment and subsidies. Total jobs are expressed as “permanent job-year equivalents.” For this calculation, construction jobs are assumed to last 2 years, whereas permanent jobs are assumed to last 10 years.

Table 15

Job-years created by CHIPS Act projects and subsidy per job-year

Construction jobs	92,980 jobs
Permanent jobs	42,715 jobs
Permanent job-year equivalents	613,110 job-year equivalents
Federal subsidies	\$113 billion
Federal subsidies per job-year	\$184,746
State subsidies	\$18 billion
State subsidies per job-year	\$29,454

Notes: Permanent job-year equivalents are calculated assuming construction jobs last two years while permanent jobs last ten years. When the breakdown between construction jobs and permanent jobs is not clear, a 50–50 split is assumed. Federal subsidies are based on the preliminary memorandum of terms (PMT) for Intel and other firms, not on the confirmed amounts which may differ.

Source: Authors' calculations based on data referenced in this report.

Fabs are notoriously capital-intensive. Even though subsidies typically represent a fraction of projected total construction costs, average subsidies for each calculated job-year amount to \$185,000. In April 2024 the average annual salary for US semiconductor employees was reported at about \$90,000, with a wide range from \$27,000 to \$170,000. Thus, subsidies per permanent job-year equivalent job are approximately twice the average annual salary.

SIA claims that 4.89 indirect jobs are created for each foundry job. Adding indirect jobs to direct jobs would sharply decrease the subsidy cost per job-year. But there is no evidence that indirect jobs created by each foundry job are greater than indirect jobs created by other industries that might have been stimulated by equivalent subsidies.

Given these hard economic facts, job creation must be viewed as a “make weight” argument for the CHIPS Act. Devoting the same funding to almost any other employment program would have created far more well-paying jobs. Indeed, that is a central criticism of the CHIPS Act by *Good Jobs First*, a public-interest nongovernmental organization. Moreover, foundry jobs require high skills and are not the sort of employment best suited for workers without technical or college training. For these workers, the construction jobs created by the CHIPS Act, about 30 percent of total job-year equivalents, are most relevant.

From the perspective of individual states—such as Arizona, Ohio, or Texas—the arithmetic of job creation differs from the arithmetic at a national level. If a modest state subsidy swings a much larger CHIPS Act grant, and if that entices a major semiconductor firm to locate a fab with capital costs many times the state subsidy, it is pure political win. State governors may emphasize national goals of self-sufficiency and technological leadership, but for their own political standing those are secondary to state employment gains. As table 15 shows, in instances where known state subsidies were coupled with CHIPS Act money, state subsidies averaged just \$29,000 for each permanent job-year equivalent.

BROADER INDUSTRIAL POLICY QUERIES

The CHIPS Act should largely meet its own stated goals and aspirations. However, until new chips production comes online, the extent of US import dependence will remain an open question. Additionally, reaching 20 percent of global leading-edge production by 2030 poses a significant challenge.

That said, additional inquiries are needed to evaluate whether the manner of implementing this turn toward industrial policy best serves the national interest. The turn was sparked by the cold war between the United States and China, launched in 2018 by the conflicting aspirations of Presidents Donald Trump and Xi Jinping. Since the cold war seems likely to persist for decades, it almost guarantees a long and expensive run in US industrial policy. How does semiconductor policy fit within this new geopolitical context? The following six questions probe the broader dimensions of semiconductor subsidies granted by the United States and other leading countries. Companion research to be published by Chorzempa will explore US fears over Chinese chip technology—fears now addressed through strict controls on chip exports, production, and technology.

Question 1: Did subsidies accelerate chips technology in the formative decades (1950–90)?

Answer: Yes, at least in some countries.

A simplified account of semiconductor economics suggests why subsidies often accelerated the advancement of chips technology in the formative decades. The potential scope of technological discovery is vast, as repeatedly shown by Moore's law. Discovery, however, is expensive: ever-increasing R&D must be expended to open the door to each succeeding chip innovation. To take one example from a [Congressional Research Service report](#), the cost to produce a 7 nm chip is four times the cost to produce a 45 nm chip. As another example from the same report, "it cost approximately \$51 million for a single firm to design and prototype 28nm chips in 2011 and approximately \$542 million to design and prototype 5nm chips in 2020." Moreover, with each successive wave of innovation, the human capital requirements become more demanding. The highly successful chip design firm Broadcom had 2,500 employees in 1999 shortly after it became a public company; by 2022 the number of employees reached 19,000 (but company revenue had grown more than 100 times). Finally, with each advance, the associated physical plant and equipment becomes exponentially more expensive. In 1992 a leading-edge US fab cost \$500 million; in 2020 a leading-edge fab (5 nm) cost \$5 billion; and in 2024 the TSMC 2 nm plant in Arizona is projected to cost \$20 billion.

Over time, escalating outlays for the requisite combination of R&D, human talent, and physical capital create rising barriers to entry. "Learning by doing" enables leading firms to put ever more distance between themselves and lagging firms. For the few firms that succeed, operating income before depreciation can exceed 30 percent of revenue. In other words, marginal costs of chip production are often low, and the fact that few firms succeed limits the number of competitors, meaning, as a general proposition, that chips can be priced well above marginal cost. Correspondingly, the leading firms do very well in financial terms. Between December 2022 and December 2024, the [average share price](#)

of six successful US chip firms (Broadcom, Advanced Micro Devices, Micron Technology, Lam Research, Applied Materials, and KLA) more than doubled, and Nvidia soared more than ten times.

These conditions create an industry characterized by few winners and many losers. According to the Congressional Research Service report, the United States hosts [more than 800](#) semiconductor firms, but only [15 US-based firms](#) had market capitalization exceeding \$30 billion in May 2023 and [only 6](#) had 2023 revenues exceeding \$17 billion. In theory, subsidies that enable select firms to overcome high entry barriers and join the golden, financially self-sustaining path of discovery and learning by doing can thereby accelerate chips technology. As sketches in the previous chapter show, four of the six leading jurisdictions subsidized chip firms at key junctures in the technology path, and the subsidies in question, even when modest, seemingly accelerated chips technology.

At the US industry's inception in the late 1950s and early 1960s, the Pentagon happily paid high prices to pioneering firms. But it was high volume in commercial applications, not high prices paid by the military, that created the industry's success. In the 1970s, DARPA R&D funding to advance miniaturization sparked the chip design industry. That clearly accelerated chip technology. The Sematech project in the late 1980s modestly advanced US chip manufacturing technology, which, at the time, was behind Taiwan and Korea—and still is today.

In the 1970s the Japanese government recognized that its memory chips lagged US technology. The response in 1976 was the VLSI Project, compelling cooperation between five large Japanese semiconductor firms—Fujitsu, Hitachi, Mitsubishi Electric, Nippon Electric, and Toshiba—all supported by modest subsidies (under \$1 billion). While other factors were important, the VLSI Project clearly accelerated DRAM technology, measured by number of transistors on each chip. Some US firms dropped out of the market, but Micron doubled down on DRAM technology and to this day ranks among leading memory chip firms.

In 1987 modest subsidies (under \$500 million), coupled with inducements for Morris Chang and other Taiwanese engineers to come home, enabled Taiwan to launch TSMC, the radical pure-play innovation in chip manufacturing. TSMC truly accelerated chip technology worldwide by enabling the separation of chip design (where US firms excelled) from chip manufacture (where Taiwan and South Korea excelled).

By contrast with the experience of the United States, Japan, and Taiwan, large financial subsidies were not an obvious technology accelerator in South Korea. Samsung and SK Hynix are highly innovative firms, but apart from the implicit benefits they derived from their *chaebol* status and the high-quality Korean education system, explicit government grants and loans were not a major factor before the mid-1990s—at a time when Korean firms had already captured a large share of the world memory chip market. What mattered more in the early years was a Korean research institute that brought together industry engineers and academic specialists. Much later, in the mid-1990s, the government sponsored a five-year R&D program with a \$500 million budget, but this was too small, and too late in the industry life cycle, to significantly accelerate chip technology.

Starting in the late 1950s and early 1960s, China provided generous subsidies for its chip industry, and those policies persist to this day. In addition to growing its own national champion, SMIC, China subsidized production by leading foreign

chip firms such as AMD, Mitsubishi, Qualcomm, Samsung, and TSMC. Subsidies enabled SMIC and foreign firms to produce and export large quantities of standard (legacy) chips but did not visibly accelerate chip technology.

Europe's key industrial policy between the late 1950s and early 1980s was a 17 percent tariff on chip imports. The tariff persuaded several US firms to set up ATP operations in Europe, but it did not visibly accelerate chip technology. In the 1980s Europe embarked on a series of R&D programs, coupled with support for physical plants. By far, the most innovative success, with quite modest subsidies, was the Dutch photolithography firm ASML. Today this is the frontier equipment firm, with a backlog of demand for advanced models that cost \$300 million per copy.

Question 2: Are expectations of technology acceleration reasonable for subsidies between 2020 and 2024?

Answer: Doubtful, apart from Japan.

Making a technology acceleration case for the current round of national subsidies is harder for two reasons. First, national measures are focused on shifting the location of foundries from foreign to domestic territory. Almost by definition, such subsidies are not oriented toward the technological frontier. Second, recent national R&D incentives have generally not had time to deliver results. That said, it is worth surveying major technological advances in recent years and their connection to national subsidy programs.

A literature survey highlights the following recent advances:

- EUV lithography, pioneered by ASML, has enabled the manufacture of smaller node chips—7 nm, 5 nm, 3 nm, now 2 nm, and soon 1.4 nm.
- New materials with a higher dielectric constant than silicon dioxide ([high-k dielectrics](#)) improve resistance to electric leakage at small nanometer scales. Intel, Micron, Samsung and TSMC are among firms manufacturing chips with high-k materials.
- GPUs are essential to AI centers. Nvidia [invented GPUs in 1999](#) for gaming purposes and provides the design for [over 90 percent](#) of these chips (largely manufactured by TSMC). Nvidia [continues to innovate](#) to entrench its dominant position. Google [also designs](#) GPUs, and Intel and AMD are producers along with TSMC.
- [Tensor processing units \(TPUs\)](#) were [first designed by Google](#) in 2016 and later upgraded. TPU chips are made by Broadcom and Samsung. They are used for gaming, machine learning, and AI.
- NAND flash memory chips with over 200 layers were [first made by Micron](#) in 2022. Samsung and SK Hynix make NAND chips with less than 200 layers. These chips enable huge memory storage in a small 3D space.

It is far from obvious that post-2020 subsidies already have made—or will make in the future—a significant contribution to any of these advances. But a few technology shoots can be observed amid massive subsidies for plant construction.

Starting with US subsidies, the CHIPS Act passed in August 2022 appropriated \$10 billion for [Regional Technology Hubs](#), to be spent over five years (i.e., by the end of 2027). In October 2023 the Biden administration announced first-phase implementation of the regional hubs. Some 31 sites, strategically spread across the political landscape, became “Tech Hubs Designees,” and 29 of them were named “Strategic Development Grant Recipients,” each receiving awards of approximately \$500,000 to flesh out their technology strategies. Most recipients are associations of local development officials and university departments.

Each Tech Hubs Designee was eligible to apply, by February 29, 2024, for the Tech Hubs Phase 2 NOFO. In the next phase, between 5 and 10 of the designees will be selected as “Designated Tech Hubs,” each receiving grants of \$40–\$70 million. Simple arithmetic indicates that even if 10 designees are selected, and each receives \$70 million, the total outlay will be under \$1 billion out of the \$10 billion appropriated for Regional Technology Hubs. This leaves at least \$9 billion for future awards.

Casual observers may have assumed that the Regional Technology Hubs funded in the CHIPS Act would be dedicated to semiconductor technology. Such observers learned, in the October 2023 announcement, that only 1 of the 29 Strategic Development Grant Recipients was a semiconductor project, the [Texoma Semiconductor Tech Hub](#) (Texas and Oklahoma). The other 28 Strategic Development Grant Recipients are pursuing various projects, ranging from critical minerals to climate.

Led by Southern Methodist University, the Texoma project envisages collaboration between chip firms in the two states and workforce training, especially for underserved communities. Yet even if the Texoma Semiconductor Tech Hub is selected as a Designated Tech Hub, its contribution to innovative chip technology will almost certainly be modest. The same assessment applies to future awards that name other semiconductor consortia.

Why do we say this? Three reasons. First, leading chip firms spend hundreds of millions of dollars each year on R&D, and they will continue doing so far beyond 2027. Few highly rated scientists and engineers will commit their careers to Designated Tech Hubs with a limited life when they could instead join a leading chip firm. Second, the history of recent chip innovations, summarized above, shows that nearly all of them are the product of corporate R&D, not academic departments. Basic research is essential for understanding the physics of chip technology. But the scale of effort required to translate fundamental physics into something like GPUs or the 200-layer NAND flash memory is enormous, well beyond the scope of most universities. SIA estimated that the R&D cost of developing 3 nm chips would be [\\$1 billion](#). Third, as the experience of Sematech showed, leading chip firms [strongly resist](#) sharing their frontier technology. High profit margins on frontier innovations are the industry’s lifeblood, and shared technology usually serves to attract new competitors, thereby lowering profit margins.

More promising is the National Semiconductor Technology Center (NSTC), funded to the extent of [\\$5 billion](#) under the CHIPS Act. The NSTC is a public-private consortium, managed by the Department of Commerce and NIST and involving the Departments of Defense and Energy, the National Science Foundation, and private firms that elect to join. Within NIST, the National Center

for the Advancement of Semiconductor Technology, led by CEO Deidre Hanford, [appears to be](#) the operational chief. Given the [centralized nature](#) of the NSTC, and the involvement of private firms, it stands a better chance of breakthrough technologies than the Regional Technology Hubs. As of this writing, the NSTC has [not announced](#) its main technology targets or its private sector members. However, in November 2024 one of the national centers was [slated](#) for Albany, New York, after intense lobbying by then Senate Majority Leader Chuck Schumer (D-NY).

Technology innovation from the CHIPS Act is also likely to flow from R&D awards to individual chip firms, made in the context of much larger awards for physical plants. The awards for both Intel and Samsung contain small, but important, research packages. A valid criticism of the CHIPS Act awards, now that we know that the Regional Technology Hubs will not become semiconductor innovation engines, is that much larger funds should have been dedicated to R&D for frontier technology.

Turning to post-2020 subsidies by other Big 6 jurisdictions, Japan's Rapidus and LSTC projects contrast favorably with CHIPS Act awards in advancing technology. While the Japanese projects are small compared to the US industrial policy thrust, they are focused on next-generation semiconductors. The same is true of Taiwan's new subsidy programs in response to the CHIPS Act. Taiwan sits at the apex of today's manufacturing technology but nevertheless allocated a 25 percent R&D deduction and grant money for improved process technologies in its most recent tranche of industrial support.

Like the United States, South Korea has embarked on huge construction of new foundries, centered in Yongin. And, like the United States, South Korea apparently assumes that its integrated manufacturers and design firms can carry semiconductor technology forward without new help from the government. Similarly, the European Chips Act aims (akin to the US CHIPS Act) to increase Europe's production of chips to 20 percent of global production (but not distinguishing between mature and advanced chips).

Faced with severe export controls by the United States and its allies, China is seeking to master technology for advanced chips. Data on the magnitude of Chinese R&D subsidies are not published, but the Congressional Research Service [reports this](#) vignette:

Since its establishment in 2016, People's Republic of China (PRC) chipmaker Yangtze Memory Technologies Corporation (YMTC) has developed rapidly, reportedly having received \$24 billion in subsidies from the PRC government. In November 2022, a reverse engineering firm claimed that YMTC had used a unique manufacturing approach to produce an advanced 3D NAND chip with 232 layers available in commercial products.

Given the national emphasis on AI and multiple defense applications, it is certain that Chinese chip firms, like SMIC, have teams of scientists and engineers seeking to create GPU, 2 nm, and other advanced chips. An example of their success is the [Huawei Mate 60 Pro](#) cell phone, announced in April 2024, powered by a SMIC 7 nm chip and manufactured with ASML equipment. Ironically, China is probably giving more emphasis to R&D in its subsidies than the United States.

Question 3: Will current global subsidies accelerate world or US territorial capital outlays for fabs and ATP plants?

Answer: Yes, for the United States, but too soon to know globally.

Table 3 indicates that annual world capex grew by around 60 percent between 2014 and 2018, but somewhat less between 2019 and 2023. When world capex figures for 2024 and 2025 are known, an acceleration in capex may be evident, given the burst of subsidies, but as of 2023 the pace of world capex growth was about the same as the 2014–18 period. The real test of world capex acceleration will come later. The burst of subsidies may simply bunch capex into the middle years of the 2020s.

Without faster revenue growth, prolonged acceleration of capex could leave chip firms with unwanted spare capacity. Table 1 shows no acceleration of revenue growth when the period 2019–23 is compared to the period 2014–18. AI systems may jolt the growth of revenue in the next five years. Additionally, the increasing sophistication of semiconductor design may require ever-higher capital outlays for every million dollars of additional revenue. Speculation around world capex acceleration therefore ends with an unsatisfying question mark.

More satisfying is the very dramatic acceleration of capex on US territory. Starting from small annual outlays well under \$10 billion through 2019, the prospect of CHIP Act subsidies raised US territorial capex to \$82 billion in 2022. Data collected by Chorzempa suggest that the 2023 US territorial capex figure will be even higher.²⁹ Evidently, the CHIPS Act succeeded in shifting a very large share of world capex to US territory. From the perspective of CHIPS Act sponsors, this was a clear win. Other Big 6 jurisdictions have a different view.

Question 4: Will future subsidies be required to reach and maintain a 20 percent US share of world production of advanced chips?

Answer: Probably.

Asian chip firms must amplify their US fab commitments to reach the target of 20 percent of world advanced fab capacity on US territory by 2030. CHIPS Act grants will likely be committed by early 2025, and the 25 percent investment tax credit (the largest subsidy) is set to expire at the end of 2026. Any fab launched by the expiration date can continue to claim the tax credit for construction that takes place at a later date. However, unless Congress renews the cash, loan, and tax subsidies, future incentives seem inadequate for Asian firms to expand as envisaged. Moreover, unless US fab construction costs fall sharply to levels experienced in Korea and Taiwan, market forces alone will not maintain the 20 percent share during the 2030s. The definition of *advanced chips* will evolve but, judging from Nvidia's GPU experience, not in a way that would point to lower construction costs.

Related to the issue of construction costs is the matter of operating costs. According to an August 2024 *Financial Times* report, some 40 percent of manufacturing plants supported by the Inflation Reduction Act and the

²⁹ From Census data, Chorzempa finds that capex on a category that covers all construction expense for electronics and computer manufacturing (in other words, more than chips) was \$105 billion in 2023 (private communication with Chorzempa).

CHIPS Act have been delayed by periods up to two years for various reasons, including labor shortages and weak demand. More shortages are projected when manufacturing plants start operating. Deloitte [foresees](#) a global shortage of semiconductor workers, with projected expansion of 100,000 job openings annually through 2030. SIA [projects](#) 115,000 new US semiconductor manufacturing jobs by 2030, of which 67,000 risk being unfulfilled based on current technical school and college graduation rates.

With the possible exception of China, all the Big 6 face labor shortages. US manufacturers may not be more handicapped by labor shortages than companies in East Asia and Europe. However, labor costs are foreseeably higher in the United States than in Japan, South Korea, and Taiwan. An [AI-Pro search](#) reports average annual wage costs, including all fringe benefits, for leading firms: Intel for US workers, \$80,000–\$120,000; TSMC for Taiwanese workers, \$60,000–\$90,000; Samsung for South Korean workers, \$45,000–\$70,000; and Toshiba for Japanese workers, \$40,000–\$60,000. Evidently, US firms face a wage disadvantage. Moreover, while US fabs are now building their labor force from scratch, East Asian fabs have had decades to develop efficient practices for precision jobs. Comparisons are harder for energy and water costs. But clearly the US fabs supported by the CHIPS Act will be challenged to bring their operating costs down to East Asian levels. And it seems unlikely that East Asian governments will slash their own subsidy programs.

All considered, if the 20 percent target becomes a mandate for security reasons, it will require continued large-scale federal support for a decade or longer. If the support is not forthcoming, the United States may turn to trade protection to preserve the US market for domestic producers. That, in a nutshell, is the history of the US steel industry and could soon become the experience of the US electric vehicle industry.

Question 5: Could tariff protection have boosted the US semiconductor industry as much as the CHIPS Act?

Answer: Very unlikely.

In October 2024, during his presidential campaign, [Trump said](#) that tariffs on imported semiconductors might have been a better way than subsidies to spur chip makers to build plants in the United States. In light of Trump's skepticism, some observers [questioned](#) whether the CHIPS Act would survive his presidency.³⁰ Moreover, during the last weeks of his presidency, [Biden launched](#) an investigation of Chinese “legacy” chips, opening the possibility of targeted tariffs when Trump takes office. Arithmetic suggests, however, that even 20 percent tariffs (a figure [mentioned](#) by Trump for imports from all countries) would not have bestowed as much benefit on US semiconductor production as the CHIPS Act.

In 2023 sales of chips in the US market amounted to \$70 billion (table 1, panel b). If a 20 percent tariff raised domestic chip prices by the full 20 percent,³¹ the

30 In November 2022, Speaker of the House of Representatives, Mike Johnson, said he would introduce a bill to repeal the CHIPS Act, but [he quickly reversed](#) the statement after hearing complaints from red state Congressmen.

31 Typically, tariff protection raises domestic prices by less than the tariff rate.

additional revenue on domestic sales would be \$14 billion annually (20 percent times \$70 billion). However, imported chips accounted for \$51 billion sales (table 14, panel a), so the tariff revenue on those sales, some \$10 billion, would go straight to the US Treasury, not to the coffers of domestic producers. Thus, the 20 percent tariff would only benefit US chip producers to the extent of \$4 billion annually (\$14 billion minus \$10 billion). The 20 percent difference between world and US chip prices would stimulate domestic investment, but chip producers on US territory would not have nearly the financial firepower delivered by the CHIPS Act. It would require many years before the cumulative size of tariff benefits approached the nearly \$200 billion of subsidy benefits conferred by the CHIPS Act.³²

Meanwhile, domestic chip users would be disadvantaged relative to their foreign competitors (autos, electronics, AI, etc.). As a historical lesson, the European Union's 17 percent tariff was judged a failure by Flamm in promoting the EU semiconductor industry. There is no compelling reason why a comparable tariff would prove more successful for the United States.

Question 6: If continued large-scale subsidies to the semiconductor industry become accepted US policy, what should be done differently?

Answer: Consider these alternatives.

Two facts combine to make a strong case for continued support: Other Big 6 jurisdictions provide large subsidies to the semiconductor industry, and US officials view the industry as essential to national security. Efficiency tests, along the lines of the “infant industry” argument, seem unlikely to be applied. Instead, officials may insist that the US semiconductor industry should rank first among peers, regardless of cost. If that comes to pass, they should consider four possible improvements:

- **Consult with allies.** The United States and its allies among the Big 6 (the European Union, Japan, Korea, and Taiwan) should consult on their subsidy plans well in advance of legislative enactment. Consultations might avert unwanted excess capacity. At the same time, they should give mutual guarantees on access to chip supplies in the event of market disruption (earthquakes, hostilities, pandemics, etc.). The United States and European Union already align their export controls, and the EU-US Trade and Technology Council could become a forum for collaboration on future subsidies. United States-Japan and European Union-Japan bilateral initiatives could address subsidies as well. While China would not be a member of a new “Big 5” semiconductor consulting group, the evolution of Chinese production and subsidies needs to be closely monitored.
- **Incentives to hold larger US inventories.** Further, to guard against supply chain disruption, the United States should provide tax incentives for chip suppliers and users to hold larger inventories on US territory. Additionally, FEMA should examine the utility of maintaining a rolling stock of chips used by key industries.

³² In December 2024, Department of Commerce Secretary Gina Raimondo called Trump's suggestion of replacing subsidies with tariffs a “horrific idea.”

- **Incentivize R&D more.** The United States should shift the balance of future incentives more toward R&D and less toward fab construction. In other words, more Franklin and less Hamilton. CSIS has [endorsed](#) this shift. Historically, R&D subsidies have been America's [best industrial policy](#). The CHIPS Act establishes a public-private national technology center with a multiyear budget of \$5 billion, much less than major chip companies spend annually on R&D. The United States has no special R&D tax credit for chips, in contrast to the 25 percent investment tax credit for plant outlays. The emphasis should change in favor of R&D. In fact, on August 1, 2024, House Select Committee on China chairman John Moolenaar (R-MI) and ranking Democrat Raja Krishnamoorthi (D-IL) proposed the R&D Promotion Bill, which would extend 25 percent tax credits for semiconductor design R&D.
- **More tax incentives, fewer grants.** Direct grants enable the Department of Commerce to choose winning companies and technologies, but the jury is out as to whether the government does a better job at selection than the market. It was not the government that propelled Nvidia and GPU technology to preeminence. Once the play of advanced fab construction has passed (Intel, TSMC, Samsung, GlobalFoundries, SK Hynix, Texas Instruments), future incentives should rely more on tax credits and less on cash grants.



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